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THEORETICAL AND EXPERIMENTAL STUDY ON ACTIVE POWER FILTERS FOR REACTIVE POWER COMPENSATION AND HARMONICS ELIMINATION

A THESIS
SUBMITTED TO THE COLLEGE OF ENGINEERING
UNIVERSITY OF BASRAH
IN PARTIAL FULFILLMENT OF THE
REQUIREMENTS FOR THE DEGREE OF
MASTER OF SCIENCE
IN
ELECTRICAL ENGINEERING

BY

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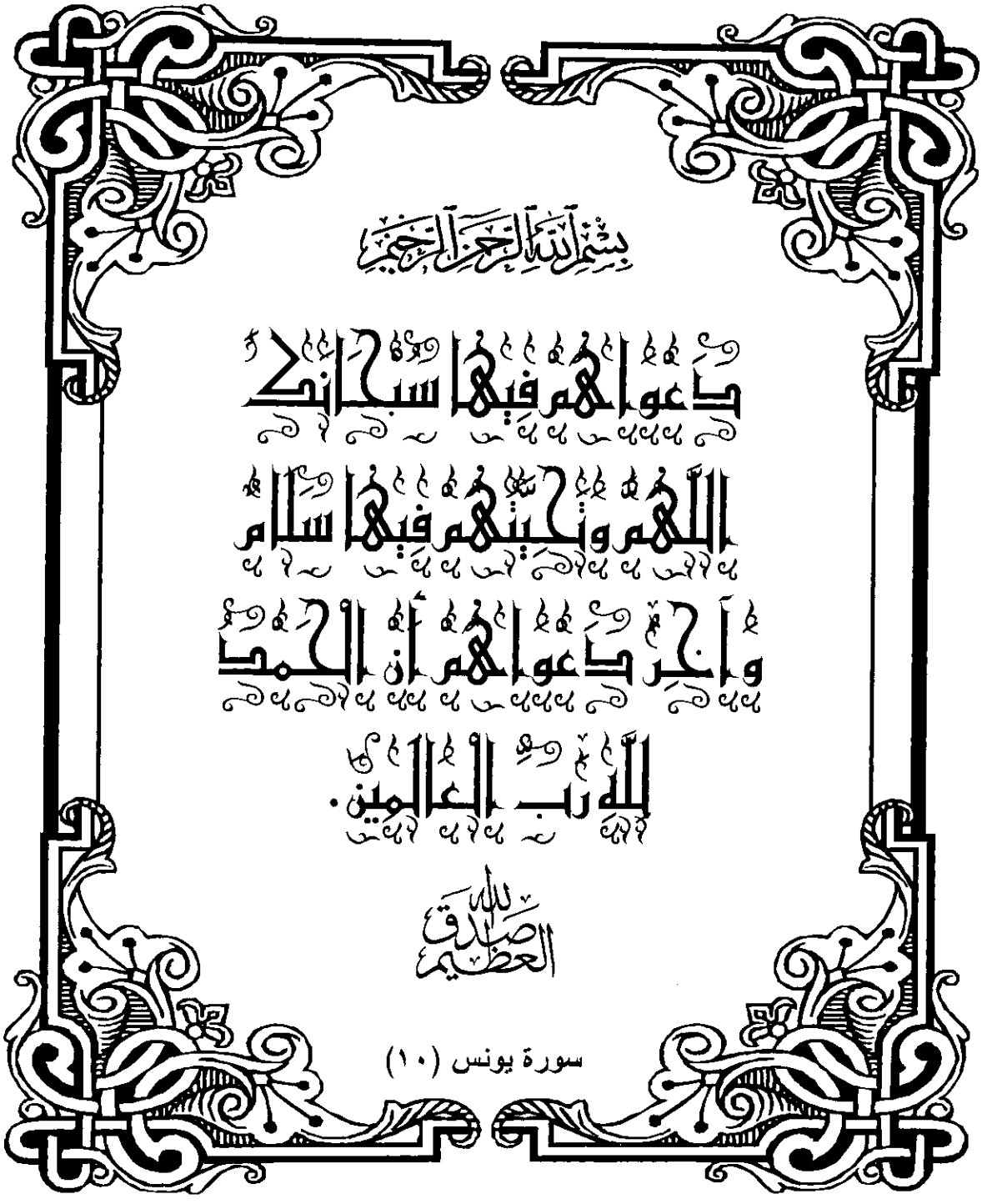
B.Sc. (ELEC. ENG.)

2001 - April


بسم الله الرحمن الرحيم
دعواهم فيها سبحانك
اللهم وتحيتهم فيها سلام
وآخر دعواهم أن الحمد
لله رب العالمين.
صدق الله العظيم
سورة يونس (١٠)

To whom
makes hearts
bleeding
before eyes.

Certification

I certify that this thesis was prepared under my supervision at the university of Basrah, as a partial fulfillment of the requirement for the degree of Master of Science in Electrical Engineering.

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(Supervisor)

Date: / /

In view of the available recommendation, I forward this thesis for debate by the examining committee.

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Committee Report

We certify that we have read this thesis, as Examining Committee, examined the student in its contents and that in our opinion it is adequate as a thesis for the degree of Master of Science in Electrical Engineering.

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Acknowledgment

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List of Symbols

$i_S(t)$	Mains current.
$v_S(t)$	Mains voltage in power circuit.
$i_L(t)$	Load current in power circuit.
$i_F(t)$	Compensating current.
V_{dc}	Voltage of dc side of the VSI.
I_{dc}	Current of dc side of the CSI.
L_F	Output inductor of the APF.
L_S	Mains inductance.
$v_{LF}(t)$	Output voltage of series APF.
$v_L(t)$	Load voltage.
$i_{FS}(t)$	Current of shunt passive filter.
$i_{rh}(t)$	Reactive and harmonic components of the load current.
$i_a(t)$	Active component of the load current.
$v_s(t)$	Mains voltage in control circuit.
$i_l(t)$	Load current in control circuit.
$i_{Sa}(t)$, $i_{Sb}(t)$, $i_{Sc}(t)$	Three-phase mains currents.
$i_{La}(t)$, $i_{Lb}(t)$, $i_{Lc}(t)$	Three-phase load currents in power circuit.
$i_{la}(t)$, $i_{lb}(t)$, $i_{lc}(t)$	Three-phase load currents in control circuit.
$i_{Fa}(t)$, $i_{Fb}(t)$, $i_{Fc}(t)$	Three-phase compensating currents.
$v_a(t)$, $v_b(t)$, $v_c(t)$	Three-phase mains voltages (line –to-neutral voltage).
$v'_a(t), v'_b(t), v'_c(t)$	Three- phase output voltages of APF.
$i_{rha}(t)$, $i_{rhb}(t)$, $i_{rhc}(t)$	Reactive and harmonic components of the three-phase load current.
τ	Width of the generated pulses

T_s	Periode of the triangular carrier signal.
A_c	Peak value of the triangular carrier signal.
$v_{inv.}(t)$	Output voltage of the APF.
M	Modulation index.
A_r	Peak value of the reference signal.
C	Capacitor of the energy-storage element.
L	Inductor of the energy-storage element.
$i_c(t)$	Instantaneous current flowing through the dc capacitor.
Δv	Voltage fluctuation of dc capacitor.
$i_r(t)$	Reactive component of the load current.
$i_h(t)$	Odd and even harmonic components of the load current
I_a	Peak value of the active components of the load current.
I_r	Peak value of the reactive components of the load current.
I_{2n}	Peak value of the harmonic components of the load current.
I_{2m+1}	Peak value of the odd harmonic components of the load current.
ϕ_{2n}	Phase of even harmonic components of the load current.
ϕ_{2m+1}	Phase of odd harmonic components of the load current.
I_o	Dc component of the load current.
K_P	Proportional parameter of P-I controller.
K_I	Integral parameter of P-I controller.
T_o	Time constant of the LPF.
α	Scaling factor of the analogue multiplier.
I_m	Peak value of the load current.
θ	Phase shift angle between load voltage and current.

ω_o	Cut-off frequency of the LPF.
f_s	Frequency of mains voltage.
u_o	Initial value of integral part of P-I controller.
y_o	Initial value of LPF.
y	Output of LPF.
u	Output of P-I controller.
i	Counter.
h	Sample time.
t	Time.
x	Output of the first multiplier.
f_o	Free running frequency of the VCO.
f_L	Lock range frequency of the PLL.
f_c	Capture range frequency of the PLL.
ω	Frequency of the load current.

Abbreviations

TCR	Thyristor controlled reactor.
TSC	Thyristor switched capacitor.
APF	Active power filter.
VSI	Voltage source inverter.
CSI	Current source inverter.
PWM	Pulse-width modulation.
PLL	Phase –locked loop.
P-I	Proportional –integral controller.
C.T.	Current transformer.
SPWM	Sinusoidal pulse-width modulation.
LPF	Low pass filter.
VCO	Voltage controlled oscillator.
T.F	Transfer function.

Because of the essential importance of reactive power compensation and harmonic elimination and also to overcome the problems of the conventional methods in this subject, the active power filters have been researched and developed.

In this thesis, a single and three-phase active power filters have been proposed and analyzed in detail. The principle of operation is explained and the design formulas are developed and tested. The presented filter is a voltage source inverter controlled as a current source by means of a pulse-width modulation (PWM) signal.

The implemented active power filter can provide the required reactive power, in addition to harmonic elimination. All the aforementioned functions (which include power factor correction and harmonics cancellation) are achieved by controlling the ac output current of the PWM inverter regardless of load type or mains voltage distortions.

A simple, effective and low implementation cost control strategy has been described. This method has only one load current sensor. It responds very fast under sudden changes in load conditions, reaching its steady state in about two cycles of the fundamental. This circuit can work properly in the continuos range of frequencies from 40 to 60 Hz by using a phase –locked loop (PLL) circuit.

Also, in this work the control laws for the filter have been derived and effectiveness of the new topology has been confirmed by both computer simulations and laboratory tests.

CHAPTER ONE

General Introduction

1.1 Introduction:-

Nonlinear loads connected to the supply network such as rectifier, inverter and cycloconverter generate high harmonic currents. The harmonic currents have undesirable effects, including additional losses in motors and generating units, overheating in transformers and cables and overloading of capacitors especially when harmonic currents are amplified at resonant frequency. Also, measurement of electricity meters, communication equipments, electronic control and protection systems may be affected by harmonics noise [1-7].

The harmonic distortion is not the only drawback of the nonlinear loads. Another disadvantage is the low power factor. Low power factor means excess current in a system, this generates excess copper losses, which results in poor efficiency. For the same power transmitted but at low power factor, the sectional area and size of the conductors are increased to carry more current [1], [8], [9].

Since distortion is unavoidable in a power electronic where will always be some reactive power flow, therefore, the goal of eliminating unwanted harmonics is similar to the goal of eliminating reactive power [9].

A conventional solution to harmonic compensation is the use of passive filter. However, this kind of filter is not adequate due to their inability to compensate random frequency variations in the current and also can produce series and parallel resonance with source impedance. Thereby, this problem is partially solved with help of LC passive filters [10-12].

Various types of static compensators have been proposed and implemented by many researchers [3], [13], [14]. The static compensator, which is based on the thyristor-technology, has been developed and evolved to two basic techniques:

1- Thyristor-Controlled Reactor (**TCR**).

2- Thyristor-Switched Capacitor (**TSC**).

These systems usually comprise shunt capacitors and inductors in conjunction with thyristor ON/OFF or phase controlled switches, to control current in reactive circuit elements (capacitors and inductors). These methods are called variable impedance type reactive power generators. In spite of the many advantages of static compensators circuit, however, various problems still exist. These problems are:

1- The thyristors here are used as controlling elements, which operate at low switching frequency.

2- The reactive power is provided by large energy storage components such as reactors and capacitors.

This thesis presents one of the major development recently applied, namely, the active power filter. This filter has been researched and developed to overcome problems of traditional methods. The next paragraphs introduce the results of an extensive survey on the subject of active power filters.

The **active power filter (APF)** connected to any linear or nonlinear loads is more interesting solution because it works as current source, that generates the load harmonic currents. Hence, the mains only needs to supply the fundamental current, avoiding contamination problems. This is the basic operating principle of an APF [15-27].

The APF uses an inverter and a dc source to generate the required voltage or current waveform. This APF can be operated with two general types of inverter; voltage source inverter (**VSI**) or current source inverter (**CSI**) as shown in Figs. (1-1) and (1-2) respectively. The dc source of a current inverter consists of an inductor while that of a voltage inverter consists of a capacitor. Also, a separate dc source may be connected instead of the

inductor or capacitor. Generally, the voltage source inverter is preferred for the active power filter because of its lower losses [10], [18].

The active power filter can be connected in series or in parallel with the supply network as shown in Figs. (1-3) and (1-4) respectively. The series active power filter works as controllable voltage source and controls the voltage at the load node, allowing excellent regulation characteristics. The shunt passive filter is connected in parallel with the load to eliminate the fifth and seventh harmonics and also helps to partially correct the power factor [12]. On the contrary, the shunt active power filter works as a controllable current source and injects the reactive and harmonic currents demanded by the nonlinear load permitting harmonic currents cancellation and power factor improvement without using passive filter [10-12].

The optimal cancellation of the harmonics will be achieved if the filter generates the modulating (reference) current identical to the waveform of the present harmonics. The cancellation, entirely, is practically impossible but reduced harmonic distortion to a minimum acceptable level for a given condition can be achieved [4]. It is necessary to transform the reference current into a feasible one by a certain method. The compensating current has been chosen as **p**ulse-**w**idth **m**odulation (**PWM**) current.

The PWM compensating current is obtained from a dc voltage or current source by the inverter circuit. This circuit cannot be made to have the same waveform as the harmonics present in ac lines unless a high modulation frequency is employed. The proper choice of PWM method enables harmonics content of the PWM current to be equal to that of the existing harmonics [19-20].

The proposed scheme presented in this work is a shunt active power filter with a voltage source inverter operates as a current-controlled based on pulse-width modulation technique. This filter can compensate for a leading or

lagging power factor without sensing and computing the associated reactive power component. Also, it attenuates the amplitude of the harmonic current components generated by nonlinear loads.

A conventional control circuits of the APF are generally complex and hard to tune. Also, it may depend on electronic tuned filters and instantaneous power theory [11]. To overcome these disadvantages, the control circuit presented is this work has been proposed and implemented.

The new control strategy of the proposed APF generates the reference (modulating) current using accurate and simple processing circuits such as only one load current sensor, subtractor and PLL estimation circuit. Also, this method is very fast under sudden change in load condition and it operates successfully in wide range of frequencies. Therefore, this circuit gives better compensation characteristics with any connected load.

Finally, the proposed control circuit has been analyzed, simulated and experimentally implemented.

1.2 Objectives of the thesis:-

Objectives of this thesis can be summarized as: -

1-Explaining the operation principle and analyzing the proposed schemes of single and three- phase active power filter to determine their behaviors.

2-Studying a general control method to achieve compensating characteristics of active power filter connected with any loads and investigating the effect of all parameters on the time response of the circuit by means of computer simulation.

3-Testing and investigating experimentally the presented prototypes of the single and three- phase active power filters for the different loads (linear and nonlinear loads) and different power factor.

4-Comparison of the computer simulation results with that obtained experimentally to demonstrate the performance of the proposed filter.

1.3 Thesis organization: -

The thesis contains five chapters:

Chapter one deals with the theory of reactive power compensation and harmonics cancellation in single and three-phase systems and introduces the conventional compensation methods. Also, an introduction to the proposed active power filters has been presented.

Chapter two will be of interest to the detailed concept and basic configuration of the active power filter. The main circuits contained in the structure of the filter are shown. Also the treatment of sophisticated PWM technique and switching pattern of each device are included.

Chapter three gives a complete description of the proposed control circuit including details of the mathematical model and how to select the parameters. It also shows clearly the behavior of the control circuit with any load (linear and nonlinear loads) and with different power factor (lagging, unity and leading) in addition to ability of this circuit in operating at a range of frequencies from 40 to 60 Hz. Also, the characteristics are verified by computer simulation.

Chapter four demonstrates experimentally the capability of the implemented active power filters to achieve the compensating performance characteristics, (which includes power-factor correction and harmonic cancellation).

Chapter five is developed for discussion and conclusion of the results and overall performance of the system. Future work suggestions are also given in this chapter.

Four appendices are included in this thesis:

Appendix (A) The 565 PLL.

Appendix (B) Selection of LPF elements.

Appendix (C) Selection of P-I controller elements.

Appendix (D) The optoisolator device.

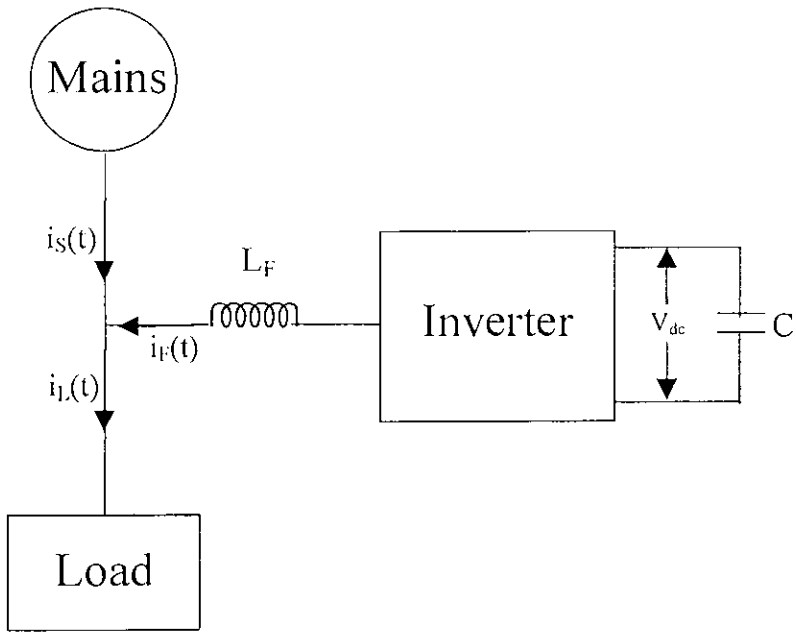


Fig. (1-1): Voltage source inverter APF.

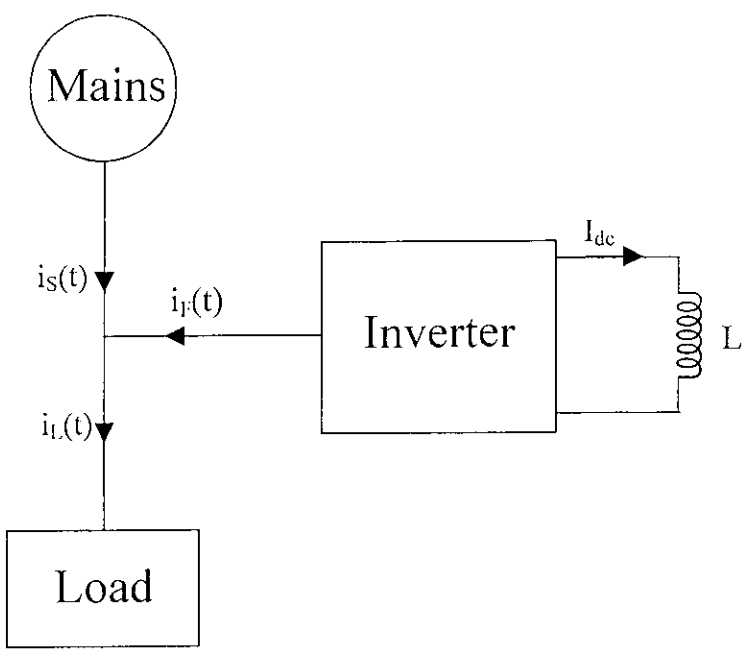


Fig.(1-2): Current source inverter APF.

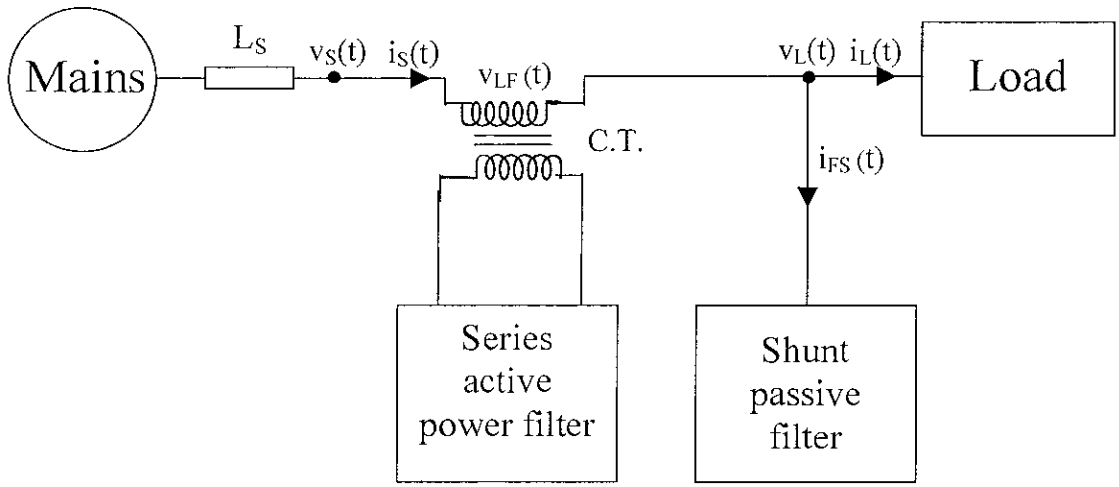


Fig.(1-3): Series active power filter.

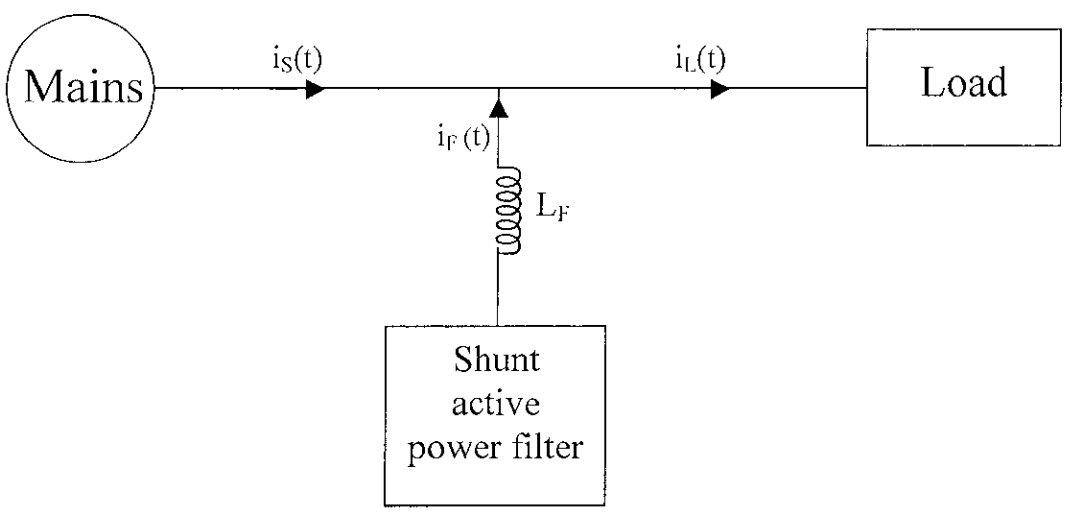


Fig.(1-4): Shunt active power filter.

CHAPTER TWO

Construction and Operation of Single and Three-Phase PMW-APFs

2.1 Introduction:-

The active power filters have been proposed as an effective solution to the growing problems of harmonic distortion and low power factor because these problems are becoming more and more importance today. The basic principle of the proposed single and three-phase active power filters can be explained by considering the filters with the configurations shown in Fig.(2-1). This figure expounds clearly a compensating theory, if the active power filter generates the compensating current (harmonics and/or reactive current demanded by the load) i_F (t), the mains needs only to supply the active current in single and three-phase system.

The performance of these filters depend on the following three basic circuits:

1- The control circuit.

2- The drive circuit.

3- The power circuit.

This chapter presents a comprehensive discussion of the basic operation of the proposed active power filters. Moreover, two types of filters will be considered in this chapter; self-controlled operation from a storage dc capacitor and an independently controlled dc supply. The design of input and output APF components and switching patterns of PWM inverter have been strictly analyzed and special attention is given to the PWM control strategy.

2.2 Basic Operation of the Active Power Filters:-

The active power filters are considered to supply the harmonics and reactive power components of the load current. Figure (2-2) shows some of the loads that act as harmonic and reactive current sources, which pollute the mains supply.

The control circuit of these filters splits the load current into two components; the active component $i_a(t)$ and the reactive and harmonic component $i_{rh}(t)$. The reference current $i_{rh}(t)$ is extracted from the load current by subtracting the estimated active component $i_a(t)$ from the load current, i.e.

$$i_{rh}(t) = i_l(t) - i_a(t) \qquad \text{----------(2-1)}$$

The obtained reference current is directly compared with a triangular carrier signal to generate the switching patterns for the inverter to produce the required injected current. This can be easily performed by the drive circuit, which will be discussed in chapter four.

Finally, the power circuit is operated according to the required switching patterns and converts a dc voltage of the voltage source inverter into PWM current that is injected into the ac lines to cancel the harmonics and compensate all the reactive power.

The general block diagrams of single and three-phase active power filters are shown in Fig.(2-3).

2.3 Power circuit description:-

The power circuit is a current–controlled, voltage source inverter (VSI) and can be studied by considering the circuit shown in Fig.(2-4). The single or three- phase voltage source inverter has an **ac** side and a **dc** side. There are two types of dc side of the inverter; storage dc capacitor or an independently controlled dc supply. Also, to reduce the current ripple and to

limit the current drawn from the APF, inductors are connected in filter branch [10][25][28]. The switching sequence of the constituting transistors of the single phase voltage source inverter can be summarized as in table 2-1:

Table 2-1: Conducting switches of single-phase voltage source inverter.

State	Conducting Switches	
1	T_1	T_4
2	T_2	T_3

From table 2-1, it can be noticed that transistors T1 and T4 are switched on simultaneously in same period, this period conducts for 180°. On the other hand, for inductive load, the load current cannot change immediately with the output voltage. Therefore if transistors T1 and T4 are switched off, the load current would continue to flow through diodes D2and D3. Similarly, when transistors T2 and T3 are switched off, the diodes D1 and D4 conduct.

A single voltage source inverters should be advanced or delayed by 120° with respect to each other in order to obtain three-phase inverters, thereby, the switching sequence of the transistors constituting these inverters can be summarized as in table 2-2[29][31]:

Table 2-2: Conducting switches of three-phase voltage source inverter.

State	Conducting switches							
1	T_1	T_6	T_3					
2		T_6	T_3	T_2				
3			T_3	T_2	T_5			
4				T_2	T_5	T_4		
5					T_5	T_4	T_1	
6						T_4	T_1	T_6

The diodes (D1-D6) conduct in the same manner as those in the single phase active power filter.

The switching patterns for single and three-phase voltage source inverters are shown in Fig.(2-5).

2.4 The PWM strategy: -

There are various techniques used to control and vary the magnitude and frequency for the inverter output. The most efficient method is the pulse-width modulation (PWM) and it is commonly used with following techniques:

1- Variable dc link.

2- Single phase modulation.

3- Multi-pulse modulation.

4- Multi-pulse, selected notching modulation,

5- Sinusoidal pulse-width modulation (SPWM).

Many references have discussed and evaluated the performance of these modulation techniques (see for example [30], [31]). The basic principle of the SPWM technique has been utilized to generate the required harmonics and the reactive power components of the load current, in this technique:

1- The frequency of reference signal determines the inverter output frequency and its amplitude controls the output voltage.
2- The number of pulses per half-cycle depends on the carrier signal frequency.
3- SPWM requires a carrier of much higher frequency than the reference signal to reduce the harmonics significantly but the switching losses increase as the carrier frequency increases.

Figure (2-6) shows the PWM output waveform for a triangular carrier signal and an ideal sine wave reference signal. The maximum and minimum values of the reference signal are limited by the maximum pulse width and minimum pulse width, which in true are decided by the intersection of the triangular carrier wave and the reference signal, i.e., the area of each pulse corresponds approximately to the area under the sine wave. Therefore, PWM inverters are adopted in applications that required less distortion in the current waveform and a compromisation has to be made between reduction of harmonics and increase of loss [32][35].

2.5 The output voltage of the APF:-

The output voltage of the APF that uses the PWM technique can be related to the modulating reference current as follows:

Because of the triangles similarity shown in Fig.(2-7), we can write

$$\frac{\tau}{T_s} = \frac{i_{rh}(t)}{A_c} \qquad \text{----------(2-2)}$$

where:

τ period width of the generated pulses.

T_s period of the triangular carrier signal.

A_c peak value of the triangular carrier signal.

$i_{rh}(t)$ reference signal.

On the other hand, the dc value of the pulse in the output of the power inverter is directly proportional to the value of its duty cycles, so;

$$v_{inv.}(t) = V_{dc} \cdot \frac{\tau}{T_s} \qquad \text{----------(2-3)}$$

Using equation (2-2) into equation (2-3) yields;

$$\frac{v_{inv.}(t)}{V_{dc}} = \frac{i_{rh}(t)}{A_c} \qquad \text{----------(2-4)}$$

Then,

$$v_{inv.}(t) = \frac{V_{dc}}{A_c} \cdot i_{rh}(t)$$

$$= M.i_{rh}(t) \qquad \text{----------(2-5)}$$

where $M = \frac{V_{dc}}{A_c}$ and is called the modulation index.

It can be noticed from equation (2-5) that the desired value of the APF output voltage can be controlled by adjusting the modulation index.

2.6 The output current of the APF:-

Using the circuit of the single phase active power filter shown in Fig.(2-8), the equation that relates the proposed filter current and voltages (output voltage of the APF and the mains voltage) can be expressed as:

$$\frac{di_F(t)}{dt} = \frac{1}{L_F}(v_{inv.}(t) - v_S(t)) \qquad \text{----------(2-6)}$$

By integrating both sides of the equation (2-6), the output current of the APF will be:

$$i_F(t) = \frac{1}{L_F}\int_o^t (v_{inv.}(t) - v_S(t))\,dt \qquad \text{----------(2-7)}$$

Substituting for $v_{inv.}(t)$ from equation (2-5) into equation (2-7) yields:

$$i_F(t) = \frac{1}{L_F}\int_o^t (M.i_{rh}(t) - v_S(t))\,dt \qquad \text{----------(2-8)}$$

This current represents the injected compensating current to ac line. To study a three-phase system, it will be converted to the equivalent single phase circuit and analyzed in the same method unless it is unbalance.

Ideally, the power supplied from the mains must be equal to the real power demanded by the load and the APF supplies the reactive and the harmonic currents, i.e., no real power passes through the voltage source inverter for a lossless active power filter system. But, in practice, the internal losses such as the switching losses in the filter will be provided by the APF.

2.7 Output filter inductor:-

The inductor (L_F) connected between the shunt active power filter and mains supply is working as a first order low pass filter to cancel the harmonics generated by the pulse-width modulation technique and to limit the output current of the APF. The value of this inductor must be small (5mH) to reduce the voltage drop on it [24, 25]. In another design, the second order low pass filter may be used to cancel any selected harmonic by connecting a capacitor across the filter in addition to the inductor [23].

2.8 The dc source of the APF:-

As mentioned in the previous sections, there are two types of dc source for the APF; the first is the self-controlled storage capacitor and the second is

the independently controlled source. In the first type, as shown in Fig.(2-9), there is a need to choose the suitable value of the storage capacitor since the dc voltage ripple and fluctuation depend on this capacitor. The value of this capacitor is determined as follows:

$$C = \frac{1}{\Delta v}\int_{t_1}^{t_2} i_c(t)\cdot dt \qquad \text{----------(2-9)}$$

where:

t_1 initial value.

t_2 final value.

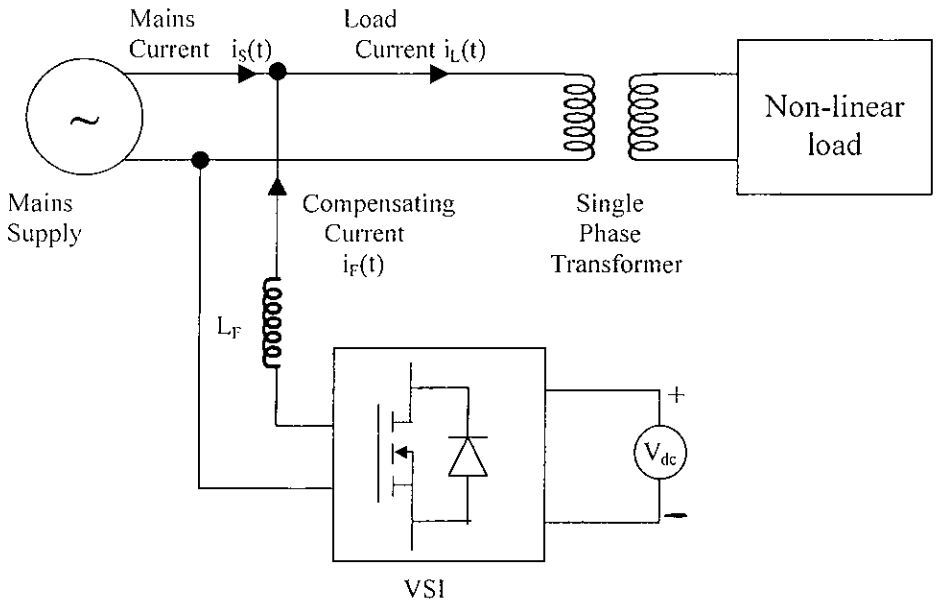
Where i_c (t) is the instantaneous current flowing through the dc capacitor and Δv is the voltage fluctuation of the dc supply [2][24-26].

Figure (2.3) shows the second type of APF where the dc side is a separate dc supply. The dc supply provides the required constant dc voltage and the real power necessary to cover the losses of the power circuit [25].

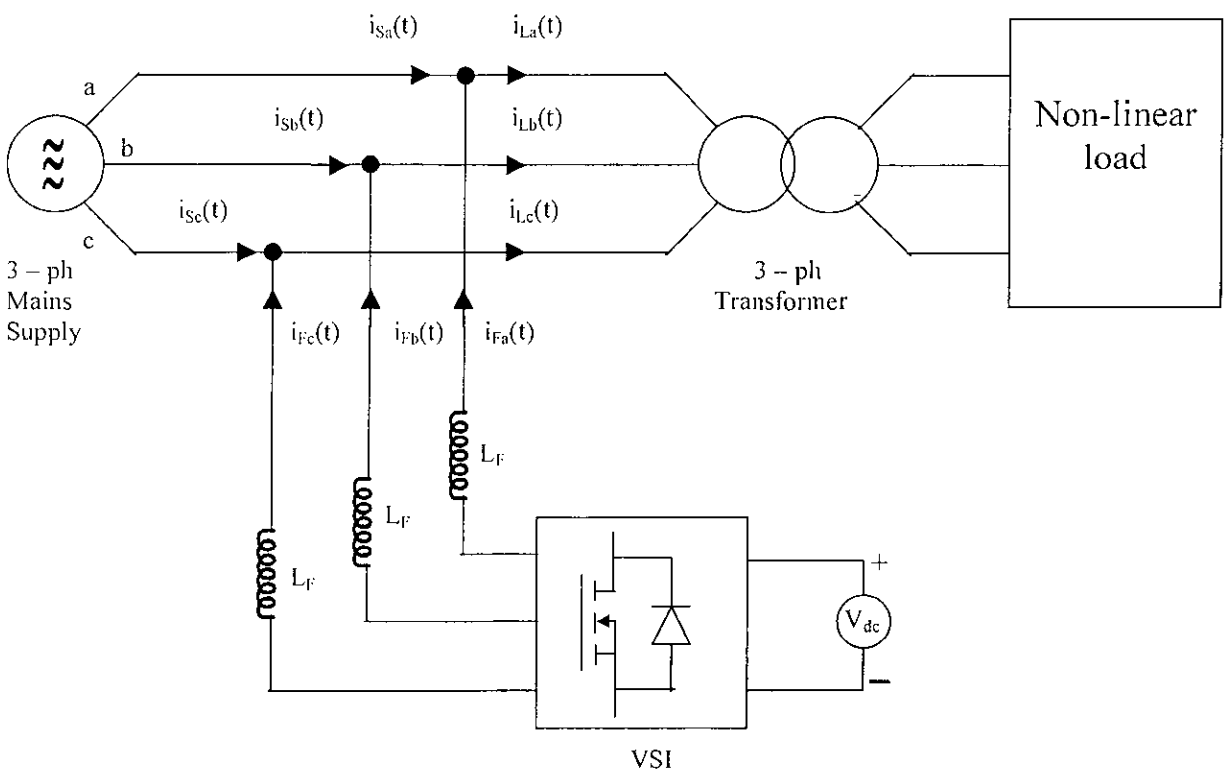
2.9 Conclusions:-

In order to deal with the major functions of power factor correction and harmonics elimination in a practical method, a compensating theory by single and three-phase active power filters is clearly expounded in this chapter.

Also, this chapter has presented a description of the PWM strategy used in the control of the considered active power filters. Moreover, the characteristic equations of the inverter output voltage and current have been derived and related to the modulating waveform.



(a)



(b)

Fig. (2-1): Basic compensation principle
(a) Single phase system.
(b) Three-phase system.

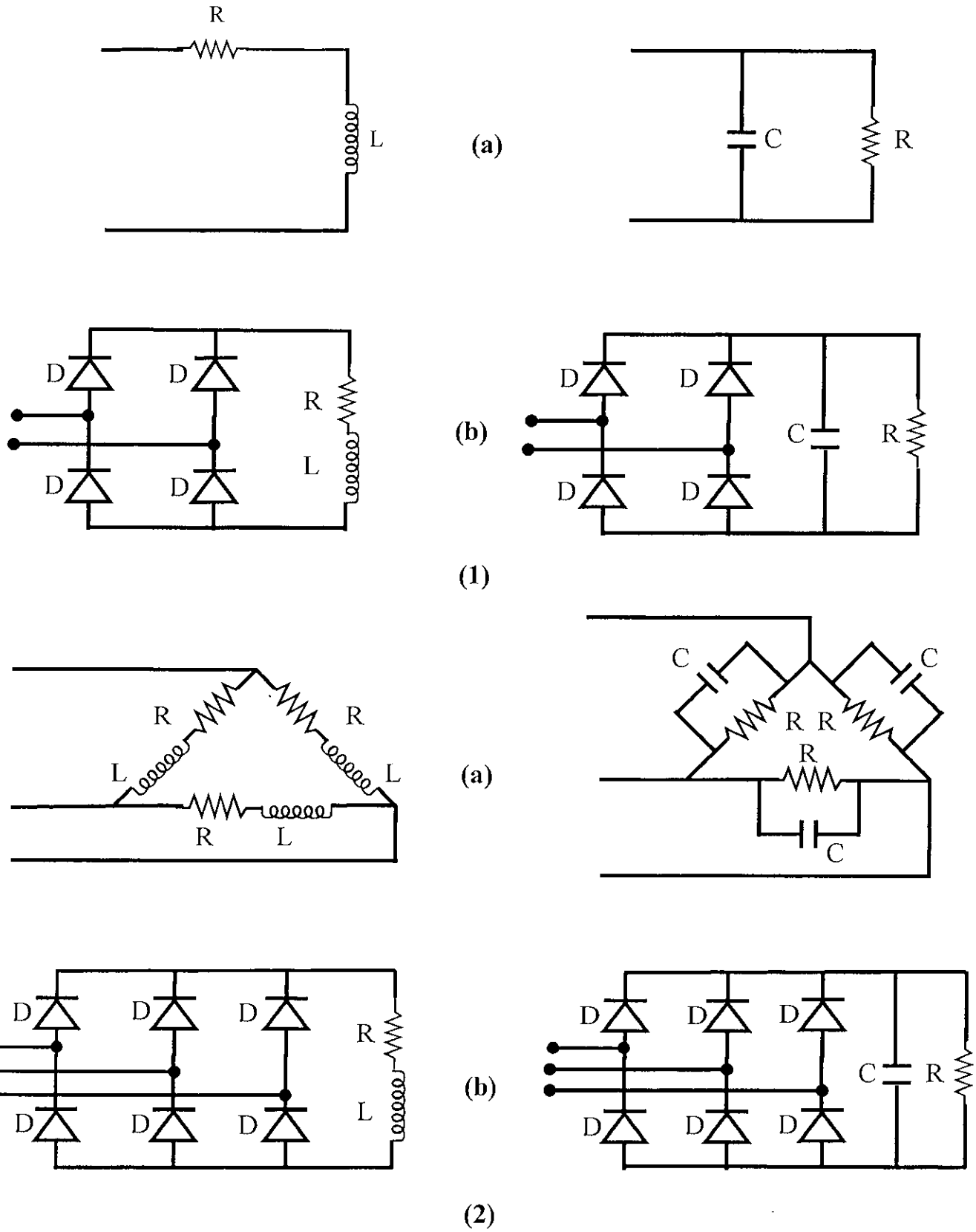


Fig. (2 – 2): (1) Single phase loads.
(2) Three-phase loads.
(a) Linear load (b) Non-linear load

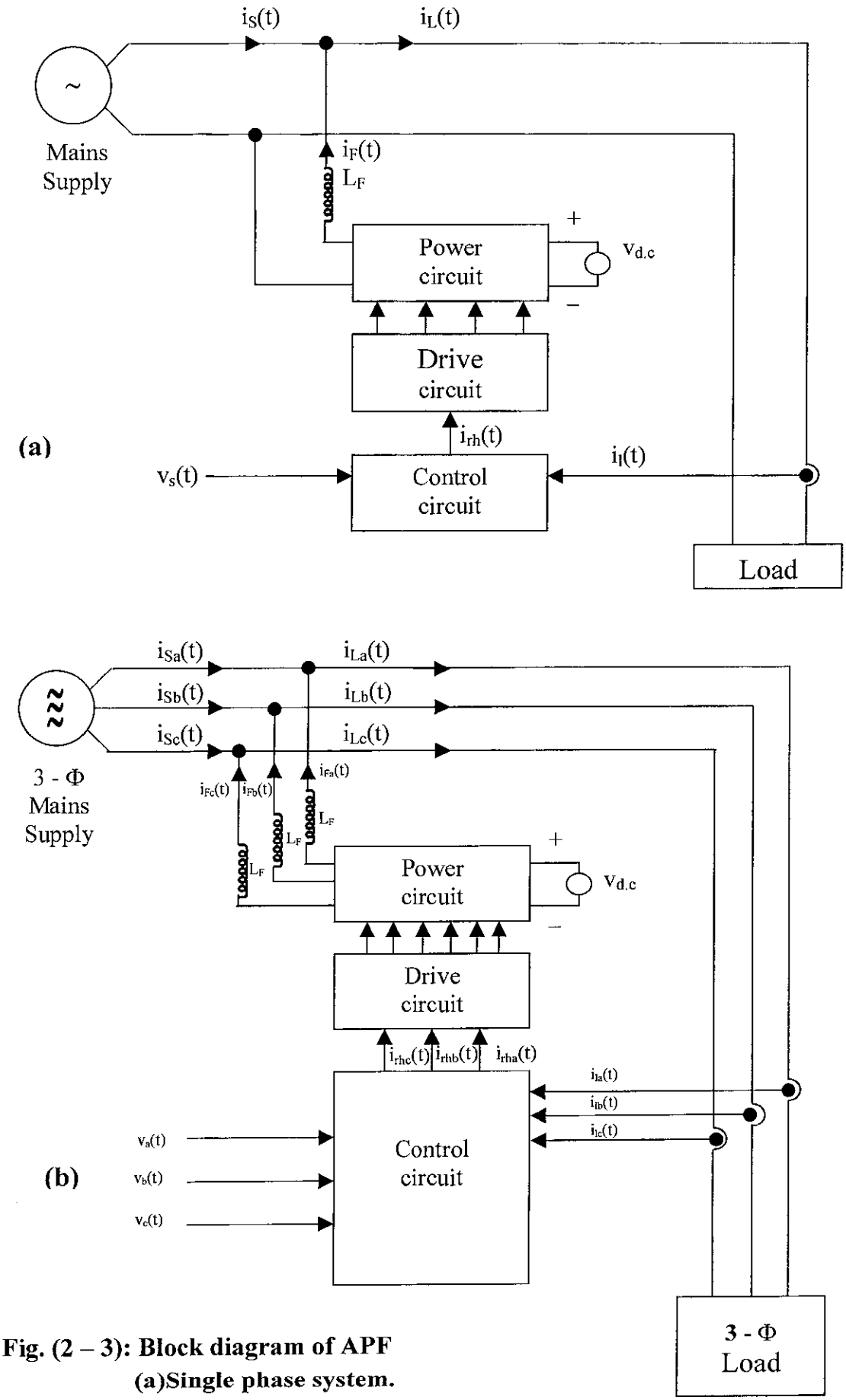
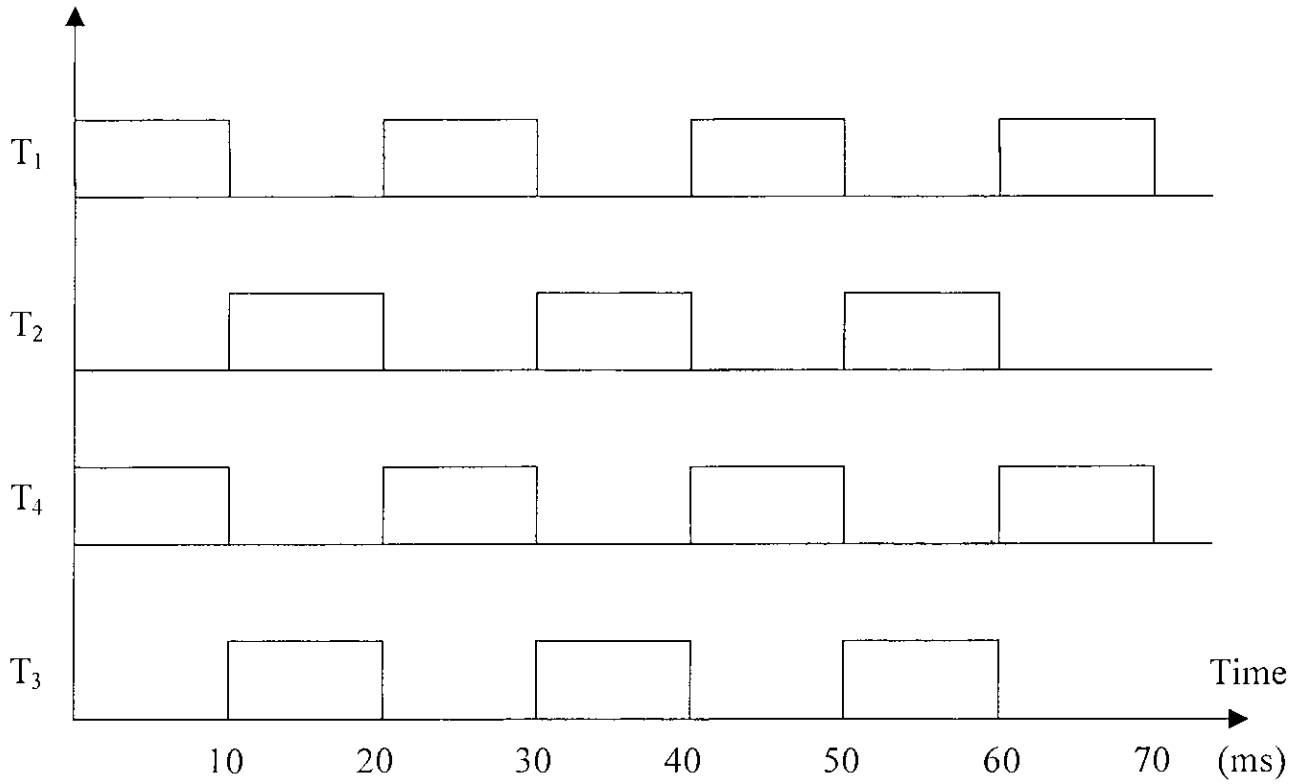
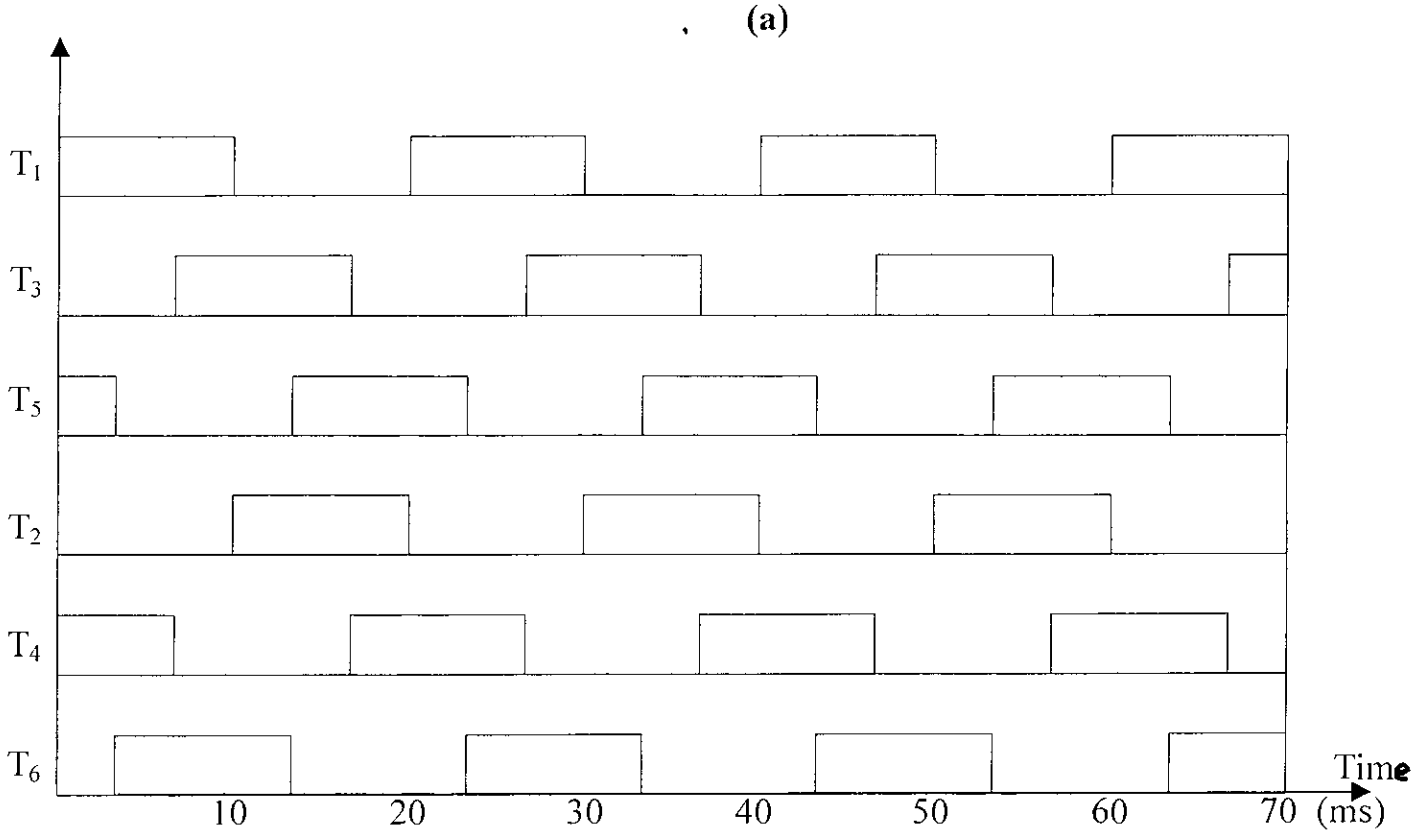


Fig. (2 – 3): Block diagram of APF
(a)Single phase system.
(b)Three-phase system.



(a)

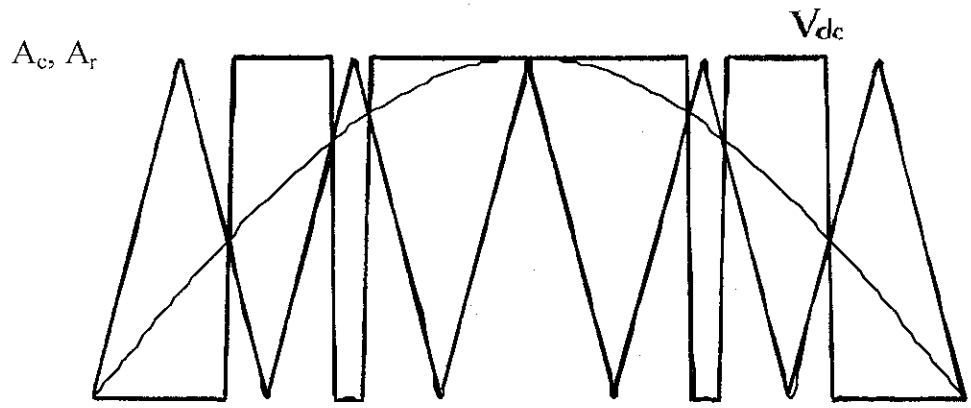


(b)

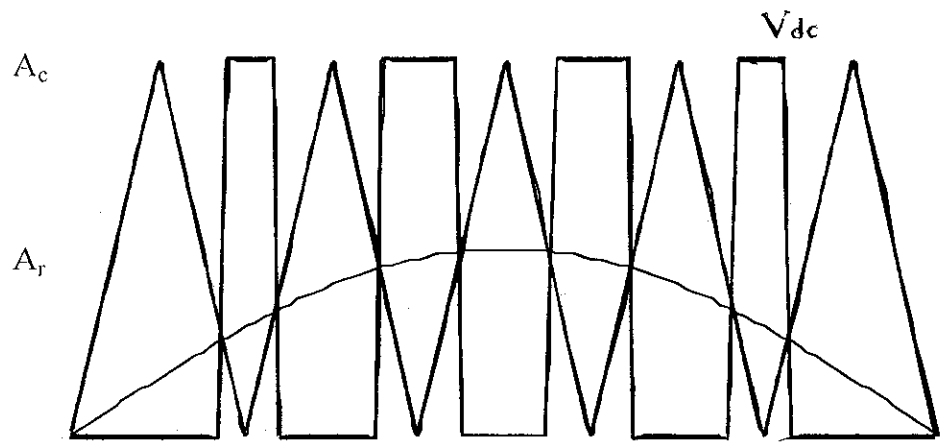
Fig.(2 – 5): Switching patterns (f = 50 Hz)

(a) Single phase inverter.

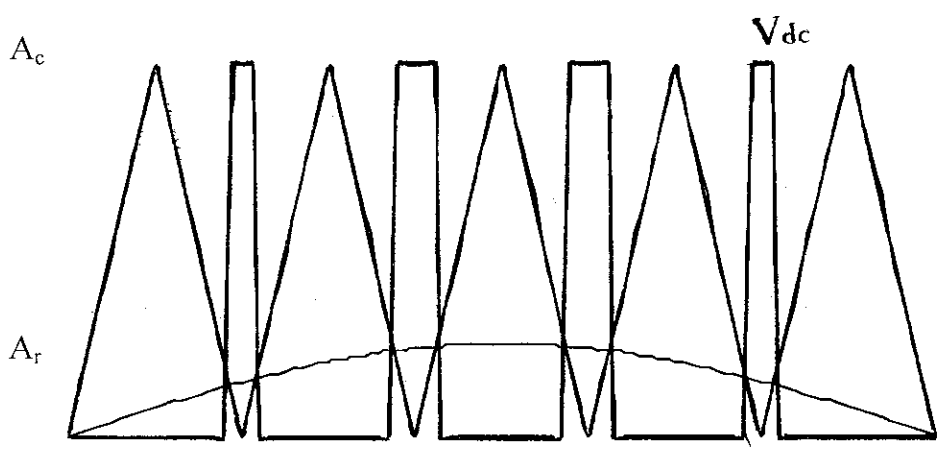
(b) Three-phase inverter.



(a)



(b)



(c)

Fig.(2-6): PWM waveform for

(a) $\frac{A_r}{A_c}=1$ **(b)** $\frac{A_r}{A_c}=\frac{1}{2}$ **(c)** $\frac{A_r}{A_c}=\frac{1}{4}$

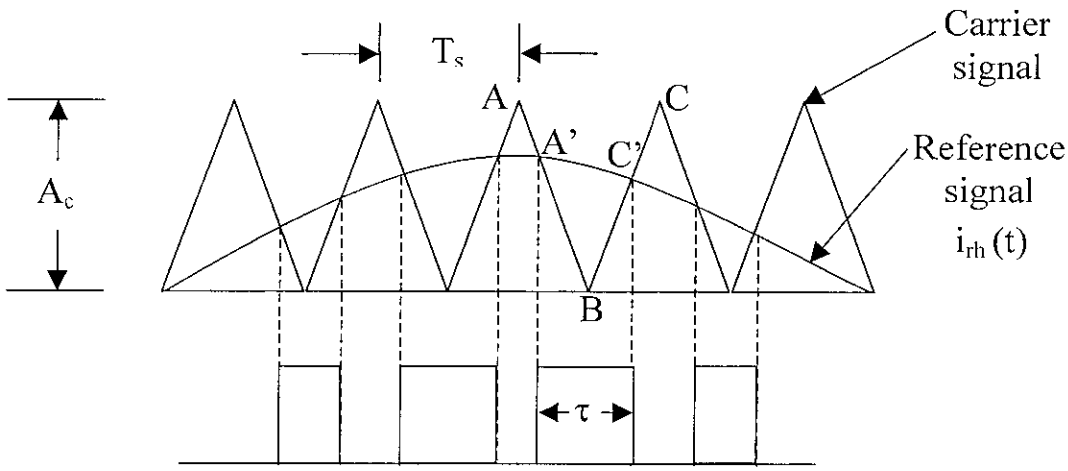


Fig.(2-7): Time diagram illustrating the PWM strategy

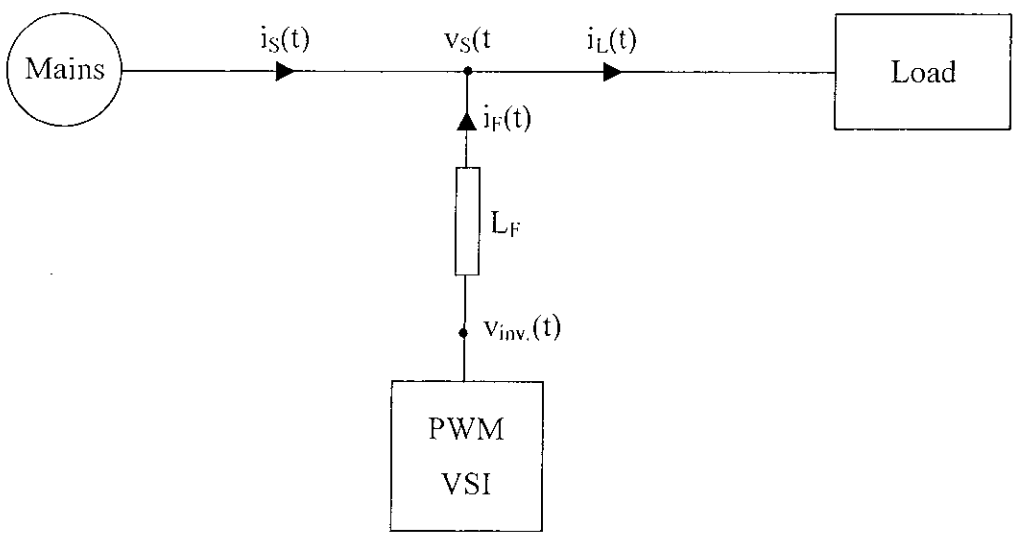


Fig.(2-8): The single phase PWM – VSI active power filter.

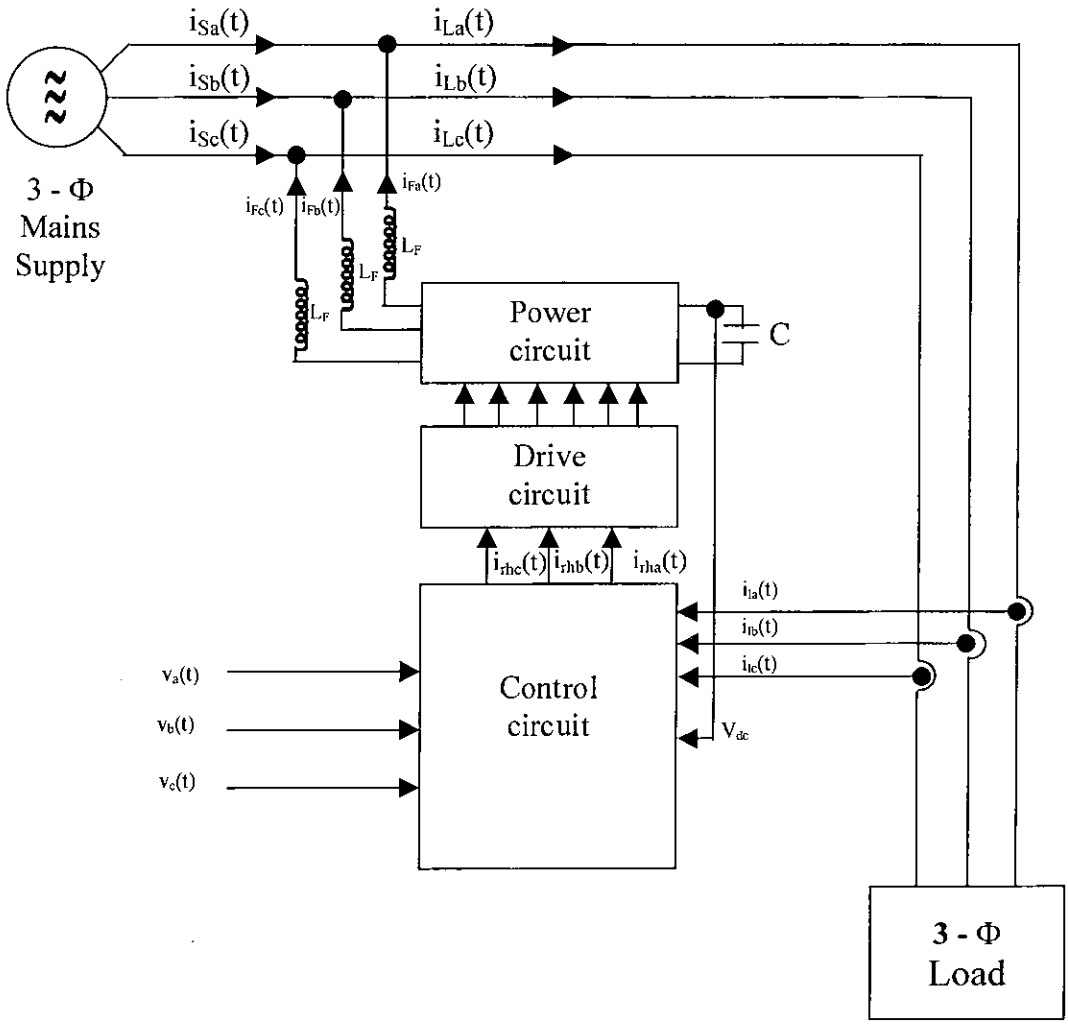


Fig. (2 – 9): Block diagram of three-phase self-controlled APF.

4.1 Introduction: -

The main objectives of the PWM-VSI active power filters considered in this chapter are:

1- Power factor correction.

2- Harmonics cancellation.

To demonstrate the capability of APF based on PWM-VSI to justify these objectives, laboratory prototype has been designed and implemented.

The implemented APFs have been tested for various linear and nonlinear loads. The linear loads include inductive and capacitive loads with different power factors, whereas the nonlinear load is considered by a rectifier fed dc load.

The current and voltage waveforms of the designed circuits (control, derive and power circuit) have been pictured at different nodes to illustrate the performance of these circuits. Then, their waveforms are compared with those theoretically obtained.

4.2 Practical realization of the single and three-phase APF: -

Figure (2-1) shows a general scheme of the single and three-phase system (mains, load and compensator). The operation of these systems is summarized by supplying the load with active power from the mains, while harmonics and reactive power are injected by the compensator.

Harmonics and reactive power demanded by the load are calculated by subtracting the estimated active current $i_a(t)$ from the measured load current $i_l(t)$. This function is achieved by the control circuit. Then, it will be compared with triangular wave to obtain the suitable pulses. Pulse-width modulation strategy has been used to improve the performance of the system. These pulses will be amplified and applied directly to each transistor in the

Finally, from analysis of the performance and practical results, it can be observed that the presented scheme has advantages of the conventional active power filter and overcome their problems.

5.2 Suggestions for future work:-

The following ideas may be suggested for future works in field of APFs

1-The high switching frequency in PWM technique increases the loss of the inverter, therefor to improve the output and avoid switching loses zero-voltage switching (ZVS) theory may be used to achieve this task.

2-A voltage feedback loop may be added to the control circuit to make a compromization between the voltage level and power factor value.

3-In this work, the active power filter based on voltage source inverter has been presented, the another type based on current source inverter (i.e., it uses an inductor in stead of capacitor in dc side of the power circuit) may be studied.

4-The control circuit may be developed by using a fully digital control of the controlled active power filter

5.1 Summary and conclusions:-

In this thesis, single and three –phase active power filters have been studied and implemented. The proposed schemes employ a pulse-width modulation voltage source inverter to compensate the reactive power requirement of the load current and eliminate the harmonic contamination caused by the nonlinear loads. Hence, the supply current will be a pure sinusoidal and in-phase with the supply voltage whatever is the type of the load.

The theoretical and experimental investigations have shown that the implemented control circuit is fast and accurate in its response for all the studied cases. Also, it has been shown that the control circuit is capable of tracking (40-60)Hz in the operating frequency of the system and generating the required control pulses.

The electronic circuits used in implementation of the control circuits (such as PLL and multiplier circuits) are simple, accurate and have a fast response making an overall response time of about two cycles of the fundamental. Hence, simplicity, low cost and fast response are the main features of the implemented control circuit.

The output current of the inverter used in the active power filter has been controlled according to the reactive and harmonic content of the load current. The tests carried out on the implemented APF have shown that its output current is effective in compensating the reactive and harmonic content of the load current for all the considered types of load (linear and nonlinear with different power factor). Almost unity power factor and sinusoidal mains current has been obtained for the different types of loads used in these tests.

The close agreement between analytical and experimental results prove the validity of the analysis and the feasibility of the proposed system.

4.4 Conclusion:-

The following two main questions have been experimentally answered in this chapter; Firstly, can the proposed PWM active power filter be controlled in order to compensate for reactive power and harmonics components and secondly, what is the maximum degree of compensation? The positive answer has been easily devised from the obtained practical results, because;

1- The control circuit has satisfactorily operated in relatively wide range of frequencies (40Hz to 60Hz) for different types of load.
2- Unity power factor and harmonics elimination have been obtained for linear and nonlinear loads.
3- The control strategy has been applied successfully for the single and three-phase APF.

CHAPTER THREE

Basic Principle, Operational Characteristics and Computer Simulations of the Proposed Control Circuit of APF

2- This approach is better the compensators that are based on the concept of the electronic filters because it can operate properly in the continuos range of frequencies from 40 to 60 Hz.

3- The adopted method responds very fast under sudden changes in load conditions and is reaching its steady state in about two cycles of the fundamental when it has a proper election of parameters.

The scope of investigation of this chapter includes general description as well as the principle of operation and performance of the proposed control circuit.Other areas of investigation include the design of this circuit to produce the required characteristics. Then computer simulations are verified.

3.2 General description: -

The load current formed by the power factor and harmonics is made up of the following four terms:

$$i_l(t) = I_o + i_a(t) + i_r(t) + i_h(t) \qquad \text{---------- (3-1)}$$

where :

I_o dc component.

$i_a(t)$ active component.

$i_r(t)$ reactive component.

$i_h(t)$ odd and even harmonics component.

Equation (3-1) can be expanded as shown in equation (3-2) to show more details about the load current, i.e.,

$$i_l(t) = I_o + I_a\cos(\omega t) + I_r\sin(\omega t) + \sum_{n=1}^{\infty} I_{2n}\cos(2n\omega t + \phi_{2n}) + \sum_{m=1}^{\infty} I_{2m+1}\cos((2m+1)\omega t + \phi_{2m+1}) \qquad \text{---------- (3-2)}$$

The first term in equation (3-2) which represents the dc component is usually small or it does not exist at all. The only component that the mains should supply is the active current, which is really the second term whereas the third term ($I_r \sin\omega t$) stands for the reactive current. The other two final terms comprise the even and odd harmonic components in the load current respectively. If the active power filter supplies the required dc, reactive and harmonic currents to the load, then the mains needs only to supply the active current. The APF current be easily obtained by subtracting the active current $i_a(t)$ from the measured load current $i_l(t)$ as follows:

$$i_{rh}(t) = i_l(t) - i_a(t) = i_l(t) - I_a \cos(\omega t) \qquad \text{---------- (3-3)}$$

Where $i_{rh}(t)$ clearly enough represents all the components in the load current except the active component. From equation (3-3), it can be noticed is easily that I_a is the magnitude of in-phase current (which needs to be estimated) and ($\cos\omega t$) is the sinusoid in-phase with the mains voltage. To achieve the experimental realization of equation (3-3), two sensors are needed, the first one is to detect the load current and the other to sense the mains voltage.

3.3 The proposed control strategy:-

The block diagram of the proposed control circuit for active power filter (one phase) is shown in Fig.(3-1). Multiplying the load current given in equation (3-2) by ($\cos\omega t$) results in equation (3-4):

$$\begin{aligned} i_l(t)\cdot\cos(\omega t) = {} & I_o\cos(\omega t) + \frac{I_a}{2} + \frac{I_a}{2}\cos(2\omega t) + \frac{I_r}{2}\sin(2\omega t) \\ & + \sum_{n=1}^{\infty}\frac{I_{2n}}{2}\left[\cos((2n+1)\omega t + \Phi_{2n}) + \cos((2n-1)\omega t + \Phi_{2n})\right] \\ & + \sum_{m=1}^{\infty}\frac{I_{2m+1}}{2}\left[\cos((2m+2)\omega t + \Phi_{2m+1}) + \cos((2m-2)\omega t + \Phi_{2m})\right] \end{aligned}$$

---------- (3-4)

In equation (3-4), the term $\frac{I_a}{2}$ is proportional with the magnitude of the active component and it can be extracted by using the control circuit shown in Fig. (3-1). In this circuit, the cut-off frequency of the low pass filter is chosen below the lowest frequency component of the line current. Therefore, all frequencies that are equal to or greater than (ω) will be attenuated. The complete attenuation of components (having frequencies $\geq \omega$) gives a good estimation of the active current amplitude (I_a). Then, the estimated amplitude (I_a) is multiplied by a unity sinusoid in-phase with the mains voltage to obtain an estimation of the active current $i_a(t)$.

Being estimated, the active current is fed with the measured load current to summing node to generate the required reactive and harmonics current which is called the reference current.

To analyze the circuit shown in Fig.(3-1), assume it has reached a steady state condition and the estimated active current $i_a(t)$ is an accurate representation of in-phase component in the load current.

After subtraction, the output of the summing node will be as stated in equation (3-3). Then, by definition and agreement $i_{rh}(t)$ should not have an active component because it is subtracted from the load current $i_l(t)$. After multiplication with ($\cos\omega t$), no dc component will be present, as can be observed in equation (3-4) by letting $I_a=0$. This means that the ΔI_a as shown in Fig.(3-1) will be zero, which will keep the output of the P-I controller I_a constant. Finally, the out put of the P-I controller will exactly correspond to the magnitude of the active current $i_a(t)$ if the load current not changed .

In Fig.(3-1), The method used to implement the line voltage in-phase sinusoid generator block, consists of a PLL circuit. The PLL technique has a unique phase tracking of the line voltage over operating frequency range

(40-60)Hz. Also, this circuit blocks efficiently the distortion in the line voltage and generates a clean sinusoid even if the input is a sequare wave.

3.4 Mathematical model:-

The control circuit in the previous section can be represented in s-domain as shown in Fig. (3-2 b). The open loop transfer gain of this circuit is:

$$G(S)=\frac{\alpha^2(K_P S+K_I)}{S(T_o S+1)} \qquad \text{---------- (3-5)}$$

The closed loop transfer function of the control circuit can be drived as follows:

$$I_{rh}(S) = I_l(S) - I_a(S) \qquad \text{---------- (3-6)}$$

and

$$I_a(S) = G(S) \cdot I_{rh}(S) \qquad \text{---------- (3-7)}$$

Using equations (3-6) and (3-7), the relationship between $I_a(S)$ and $I_l(S)$ can be shown to be:

$$\frac{I_a(S)}{I_l(S)}=\frac{\frac{\alpha^2 K_P}{T_o}S+\frac{\alpha^2 K_I}{T_o}}{S^2+\frac{1}{T_o}(\alpha^2 K_P+1)S+\frac{\alpha^2 K_I}{T_o}} \qquad \text{---------- (3-8)}$$

3.5 Simulation results: -

This section investigates the effect of circuit parameters on the response of the system. These parameters are determined by the iterative computer simulation. The obtained values from this test enable the designer to select the best possible response of the circuit. Further, this section studies the performance, accuracy and stability of the designed control circuit. Also, the simulated results of linear and nonlinear load tests will be introduced.

3.5.1 Selection of control circuit parameters: -

The parameters of the low pass filter, P-I controller and analogue multiplier have been selected to give a good compromise between output overshoot and settling time. Choosing the scaling factor of the analog multiplier (α) as 1V/V and the time constant of the low-pass filter (T_o) as 0.094 sec. (i.e. the cut-off frequency of 10 Hz) gives a good attenuation for frequencies equal to or greater than the mains frequency. The filtering characteristics of the low pass filter for the chosen parameters is shown in Fig.(3-3).

An improvement in the response of the closed loop circuit has been obtained by the proper choice of the P-I controller coefficients. These coefficients are determined by iterative computer simulations of the controller response for different values of K_P and K_I. The effects of the proportional parameter K_P and integral parameter K_I of the P-I controller on the response of the control circuit are illustrated in the curves of Figs.(3- 4 and 3-5) respectively. From Fig.(3-4), it is clear that optimal response of the system is obtained with $K_P = 35$. Also, the effect of the another coefficient K_I on the response is investigated using Fig.(3-5), where good stability of the system is obtained with $K_I = 400$ for the considered specifications.

Finally, the consequence of electing the optimal values for K_P and K_I as showed in Fig.(3-6). Where the response of the P-I controller reaches its steady-state value in about two cycles without any overshoot in the current amplitude.

3.5.2 The stability test: -

Using the selected values for α, T_o, K_P and K_I in equation (3-8) yields equation (3-9):

$$\frac{I_a(S)}{I_l(S)} = \frac{372.978S + 4255.32}{S^2 + 382.978S + 4255.32} \quad \text{---------- (3-9)}$$

The Routh and Herwitz criteria has been used to investigate stability of the analyzed system [36]. The characteristic equation of the closed loop transfer function is:

$$S^2 + 382.978S + 4255.32 = 0 \quad \text{---------- (3-10)}$$

Using this characteristic equation, Routh table for stability is as listed below:

Table (3-1): Routh table for stability of equation (3-10)

S^2	1	4255.32
S^1	382.978	0
S^o	4255.32	0

For stability reasons, the first column terms in table (3-1) must not change in sign, therefore the presented system is stable. Also, since equation (3-10) has only positive coefficients, then it is always stable [11].

3.5.3 Load test: -

In this section, the computer simulations were run with different types and magnitudes of the load current to check the performance of the control circuit. Simulation results show that excellent harmonic cancellation and reactive power compensation can be achieved by the designed control circuit for all the simulated cases. Figure (3-7) shows the flow chart that describes

the processes performed to simulate the operation of the control circuit for the different study cases. This control circuit has been subjected to the following simulation conditions:

(a)Chang in the magnitude of a UPF load current

Figure (3-8) shows the response of the control circuit for a change in the magnitude of the current. As it can be seen from this figure, the response of the circuit reaches its steady values in about two cycles which is given acceptable time in power system control.

For a load with unity power factor, a change in its magnitude will produce momentary harmonic current and distortion in the active current as illustrated in Figs.(3-8b and 3-8d). Also, from this figure one can conclude that the active power filter will not inject any current in power system for unity power factor and all the load current will be supplied by the mains.

(b) Change in the magnitude of the load current with different power factors

In this case, the current takes the following from:

$$i_l(t) = I_m \cos(\omega t \pm \theta) \qquad \text{---------- (3-11)}$$

The control circuit has been investigated for a change in the load current for different power factors. Figure (3-9) illustrates the key waveforms for a load current displacement of 50 lagging whereas Fig.(3-10) shows them for 50 leading. Greater phase displacement effect on the control circuit response is illustrated in Figs.(3-11 and 3-12).

Simulation results for the different phase displacements considered above show that the control circuit performs its function efficiently and the

reactive current supplied by the active filter will be increased according to the reactive component of the load current.

(c) Nonlinear load test

Now, the load current is represented as a waveform contains a fundamental plus third and fifth harmonics as shown in Fig.(3-13). Simulations of load current with high order of harmonics are illustrated in Figs.(3-14 and 3-15). The simulation results for the non-liner load show that these loads are associated with harmonics and reactive power generation by the active power filter. Also, half wave rectifier load requires that the active power filters supply the dc component of the load current as shown in Fig.(3-16).

The response of the control circuit for there loads has proved its effectiveness and validity for the harmonic and reactive power compensation.

(d) Change in the frequency of the load current

To investigate the ability of the designed control scheme in operating at frequency other than 50 Hz and giving the same characteristics as when it is working at 50 Hz, i.e., the estimated active current still sinusoid and in- phase with the mains voltage, simulations have been carried out to operate the control circuit at 40 Hz and 60 Hz mains frequency. Figures (3-17 and 3-18) have illustrated the ability of the control circuit to eliminate the harmonics and compensate the reactive power in this range of main frequency.

(e) Change in the frequency and magnitude of the load current

To subject the control to a worst case, the magnitude and frequency of the current are assumed to have changes in their values at the same time.

However, even for these worst cases; Figs.(3-18 and 3-19) show that the control circuit can perform its job efficiently.

3.6 Conclusion: -

The control circuit represents a major part of APF since the performance, complexity and cost of the filter depend mainly on its control circuit. In addition to main task of the control circuit in the reactive power compensation and harmonic cancellation, it must responds as quickly as possible for any change in its inputs without causing a serious overshoot in the circuit currents or voltages.

In this chapter, the implemented control circuit has been investigated, by simulations, for different trouble load conditions. The simulation results show that this control circuit can perform its job accurately and efficiently under all the assumed conditions such as the sudden change in the magnitude and phase of the load current, change in the operating frequency of the power system and also under the condition of linear or non linear load.

Appendices

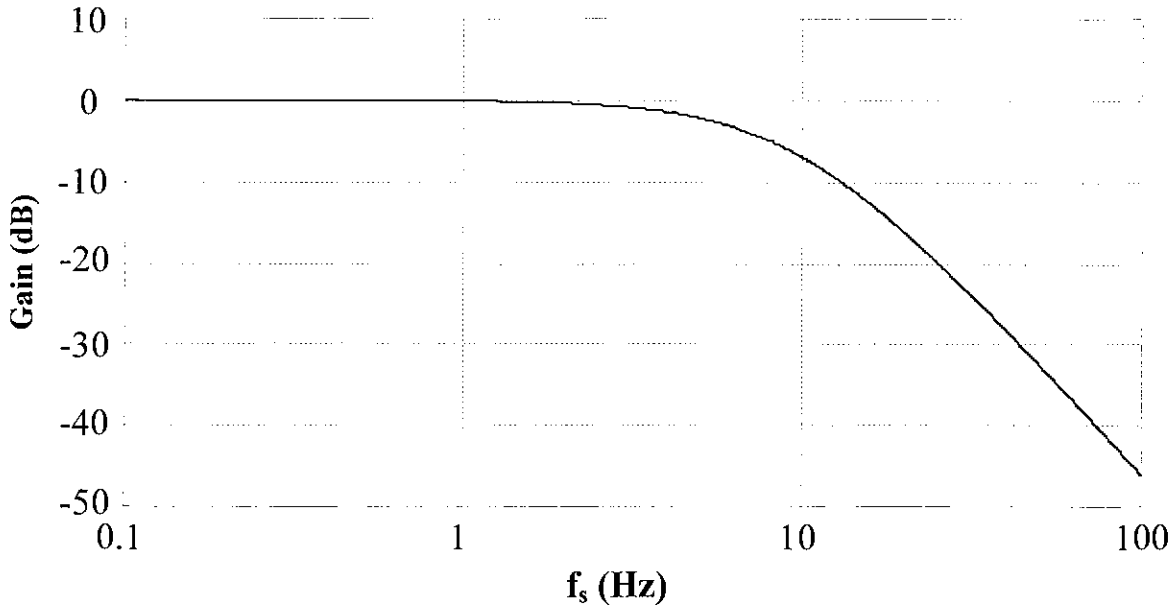


Fig.(3-3):Filtering characteristics.

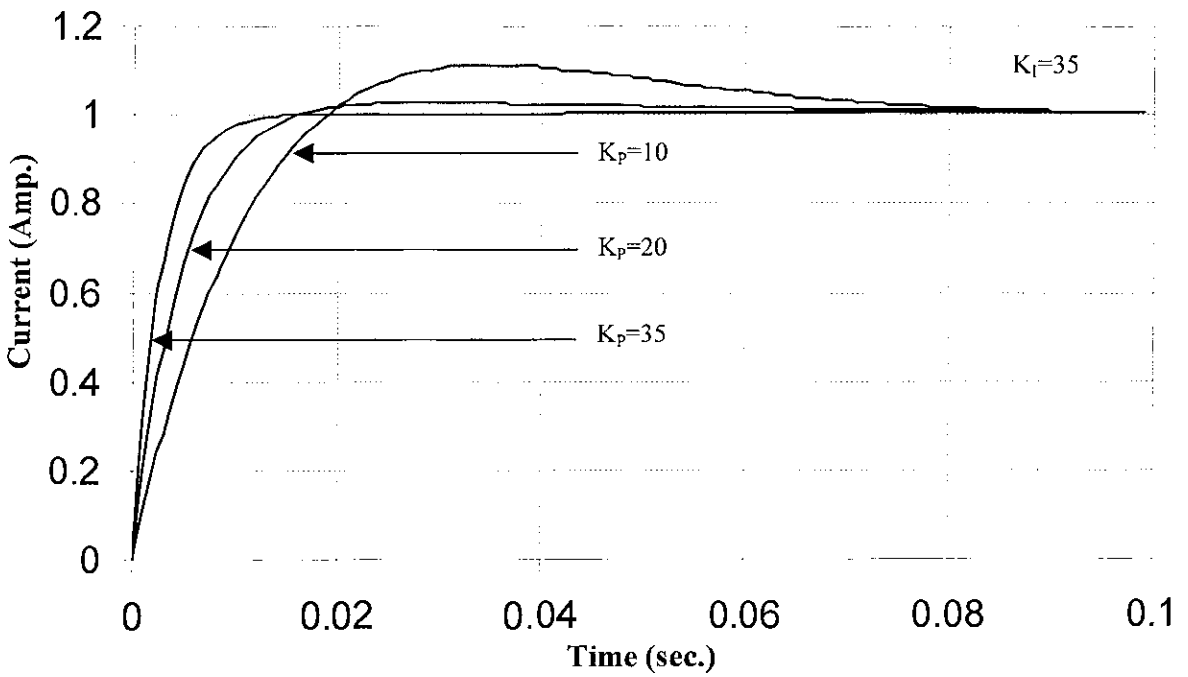


Fig.(3- 4): Response of the closed loop circuit, unit step input with variation of K_P.

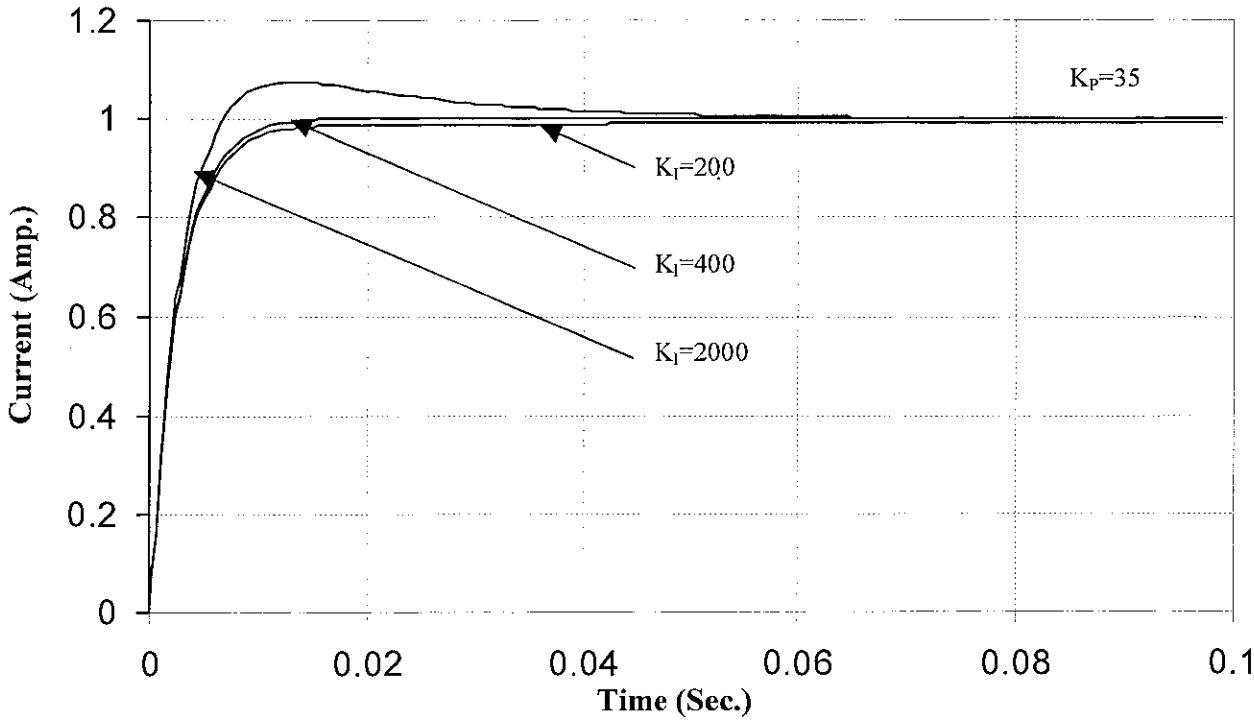


Fig.(3-5): Response of the closed loop circuit, unit step input with variation of K_I.

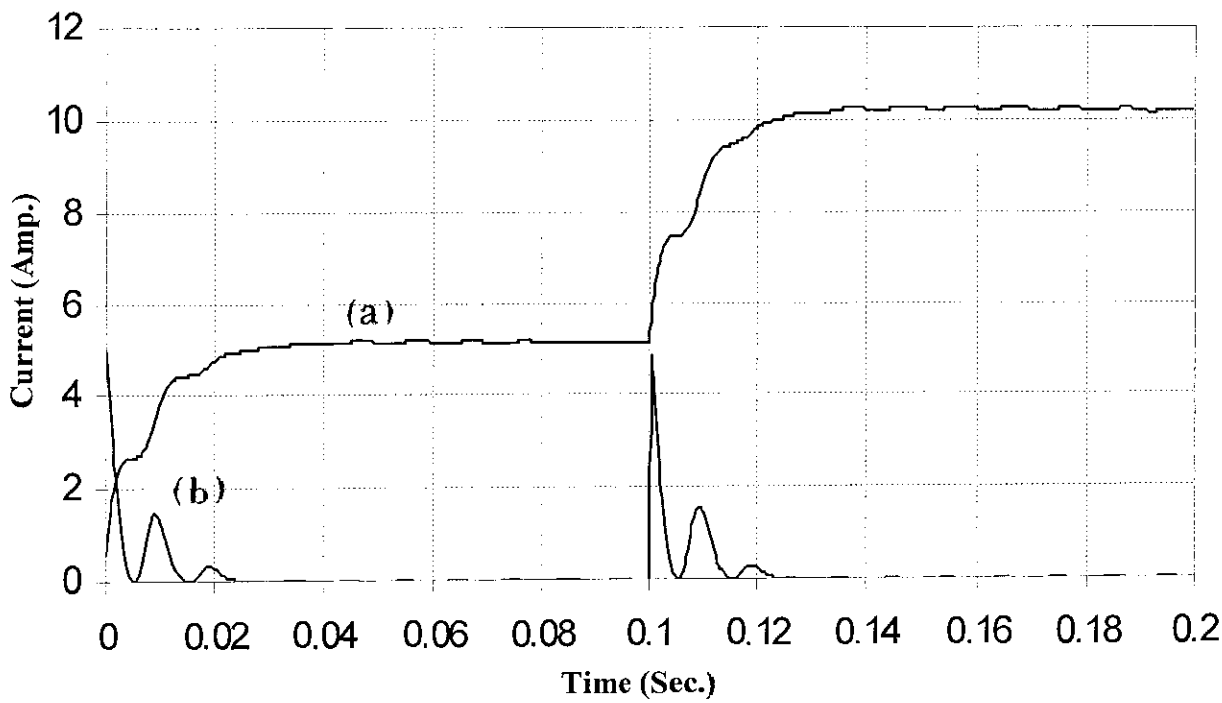
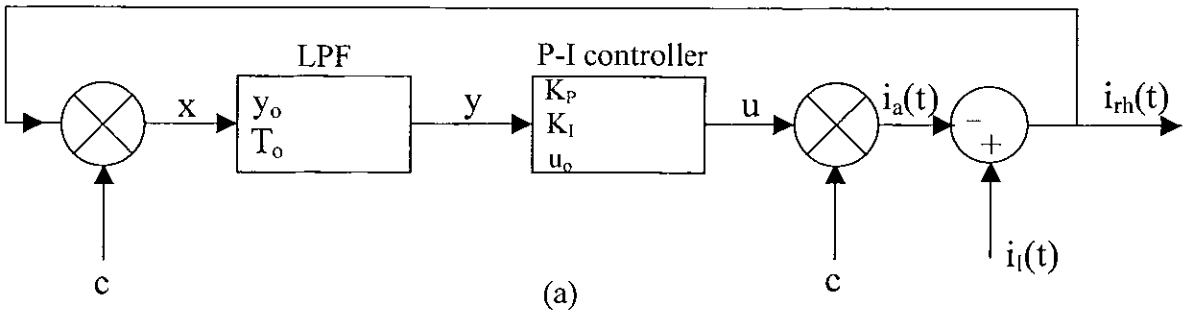
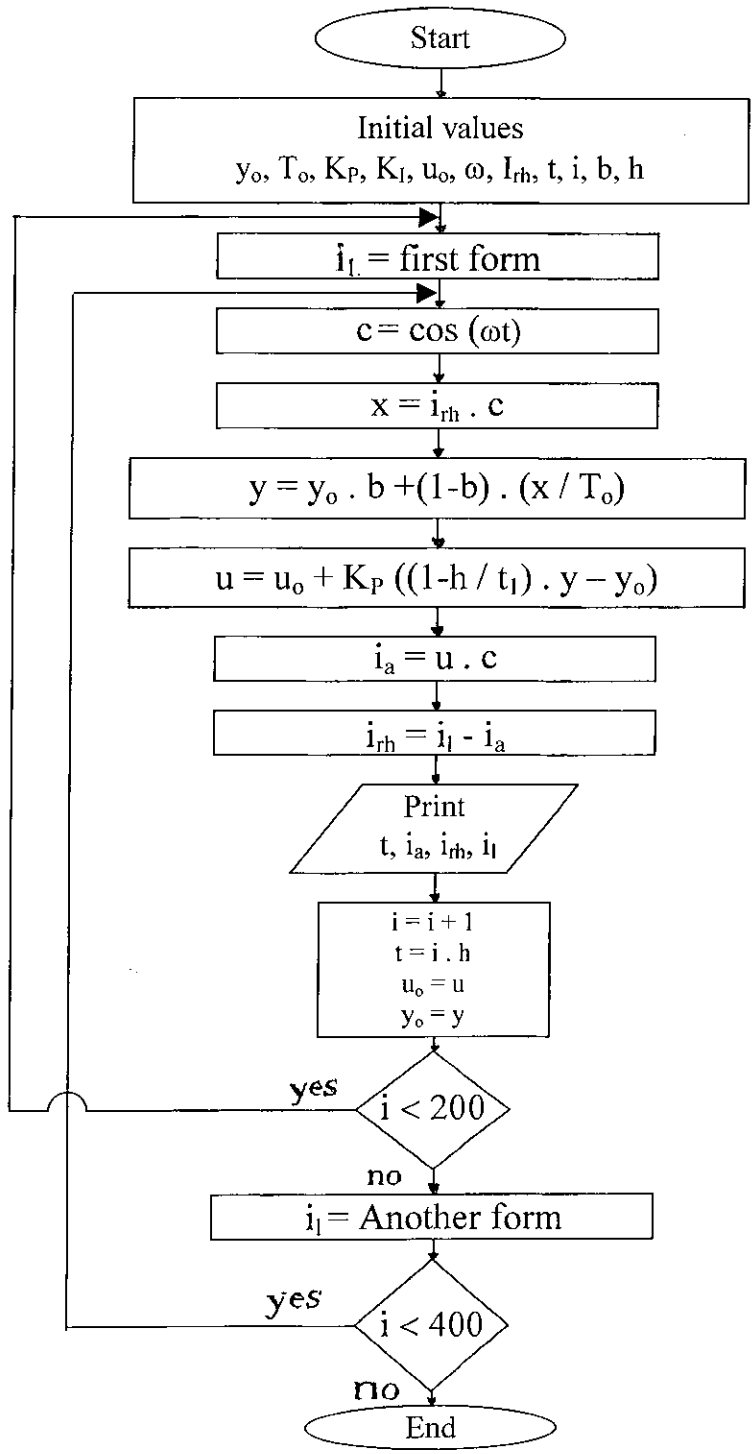


Fig.(3-6): (a) P-I controller response for current load change at unity power factor.
(b) Output of the first multiplier.



(a)



$$t_1 = K_P / K_I$$

$$b = \exp(-h/T_o)$$

(b)

Fig.(3-7): The flow-chart of main program.
(a) Closed loop control circuit.
(b) Flow-chart of program.

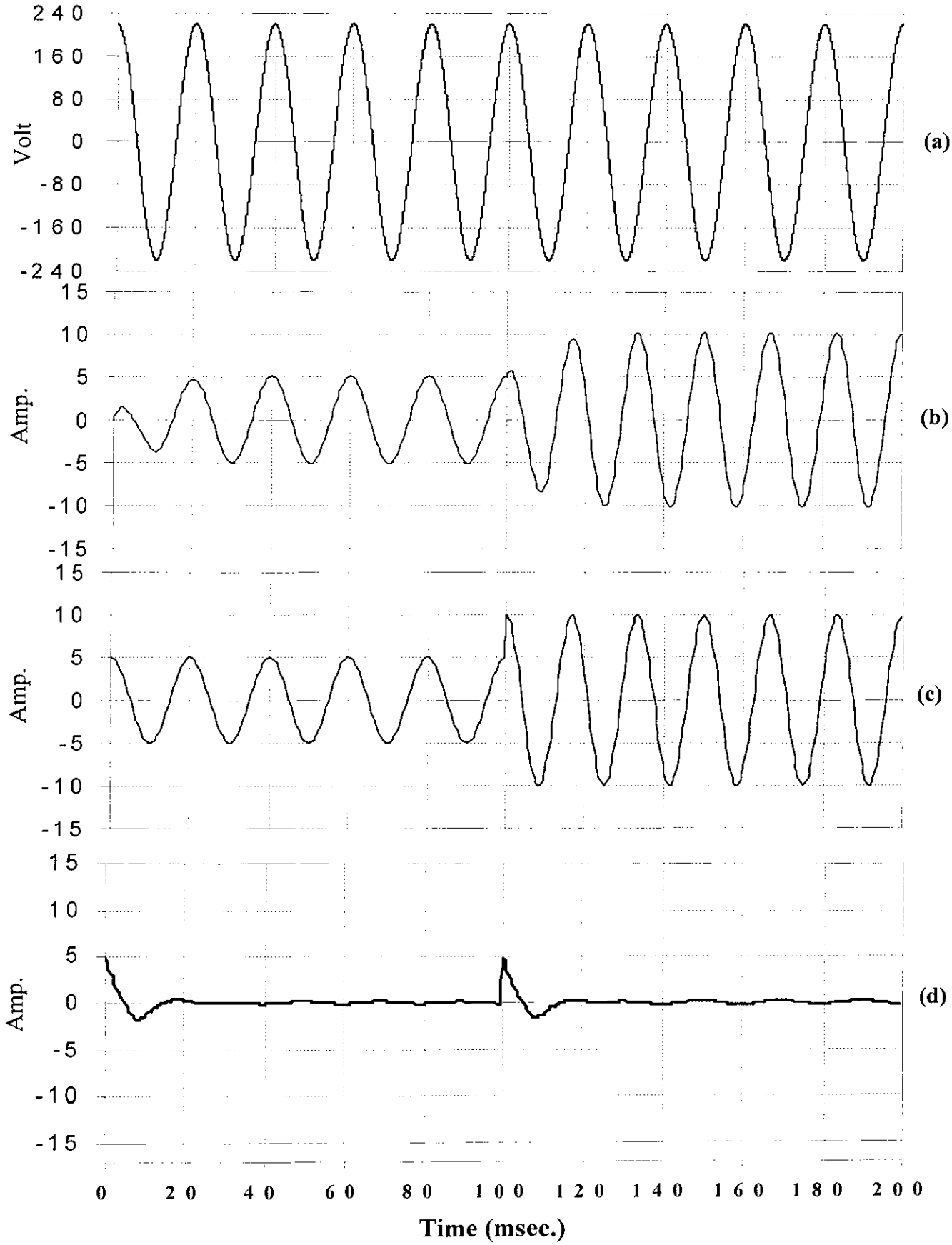


Fig.(3-8): Simulation results for $\theta=0^{\circ}$, $f_s=50$ Hz. (a) Mains voltage $v_s(t)$, (b) Estimated current $i_a(t)$, (c) Load current $i_l(t)$, (d) Reference current $i_{rh}(t)$.

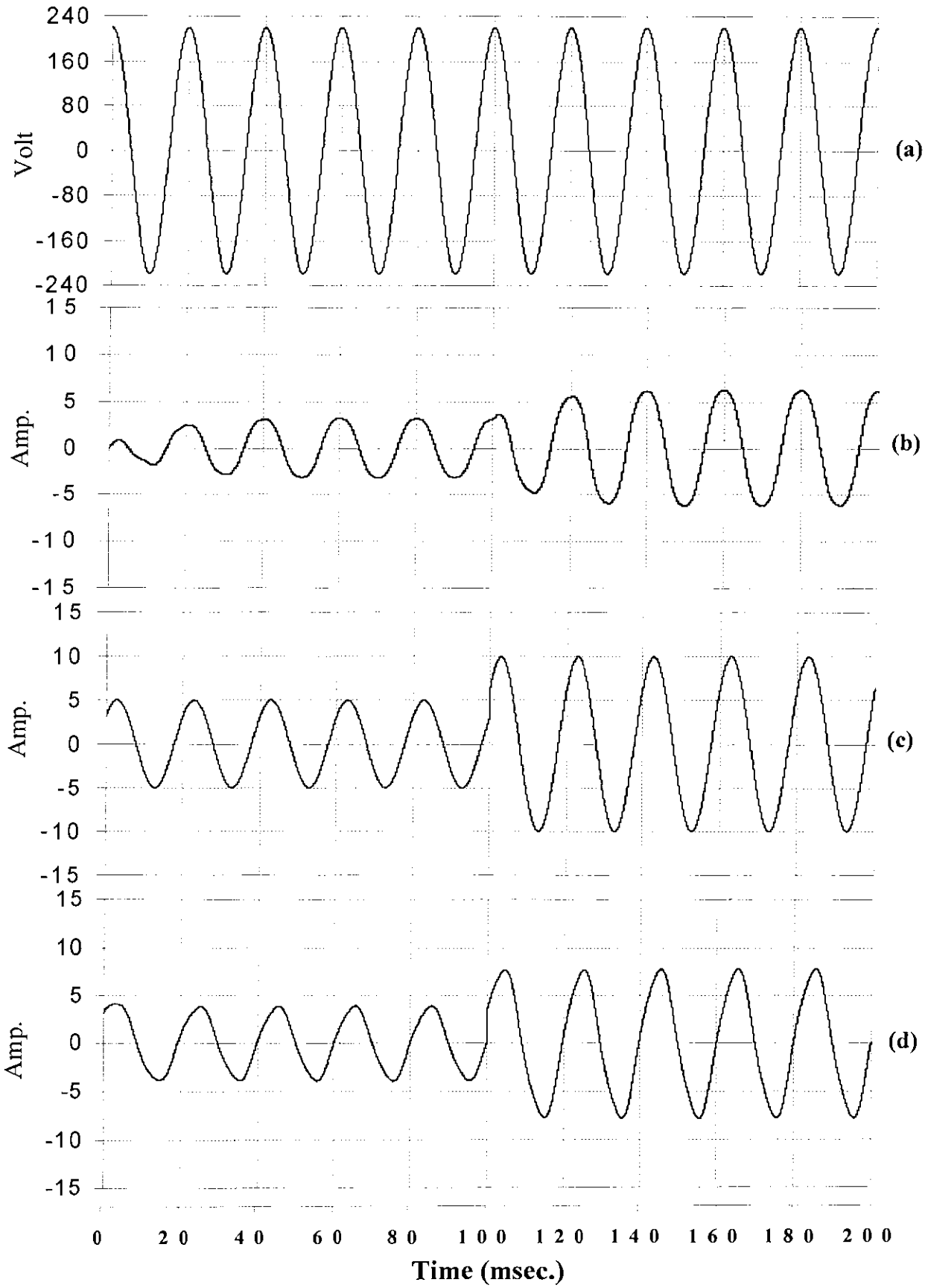


Fig.(3-9): Simulation results for θ=50° lag, f_s= 50 Hz. (a) Mains voltage $v_s(t)$, (b) Estimated current $i_a(t)$, (c) Load current $i_l(t)$, (d) Reference current $i_{rh}(t)$.

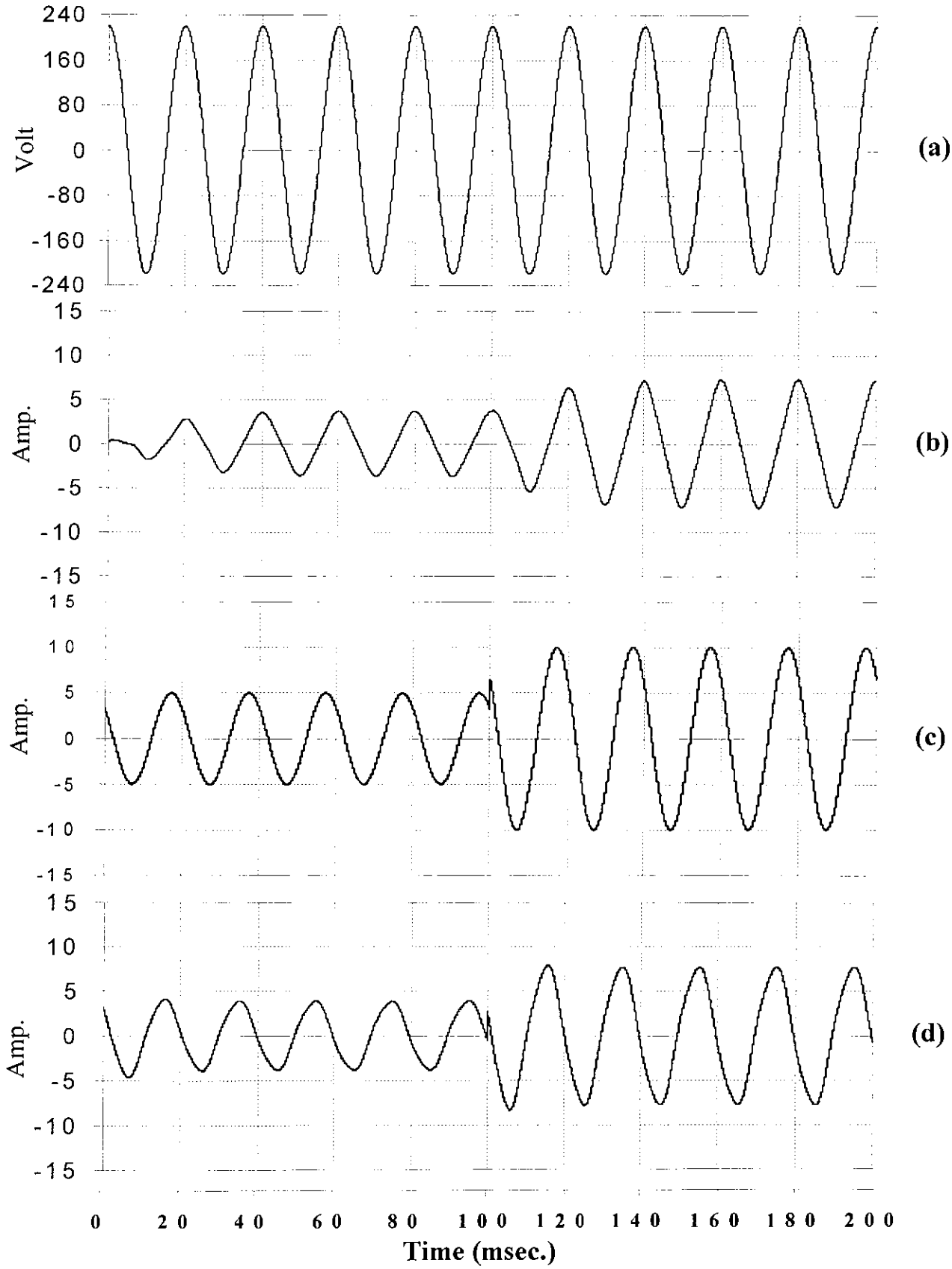


Fig.(3-10): Simulation results for θ=50° lead, f_s= 50 Hz. (a) Mains voltage $v_s(t)$, (b) Estimated current $i_a(t)$, (c) Load current $i_l(t)$, (d) Reference current $i_{rh}(t)$.

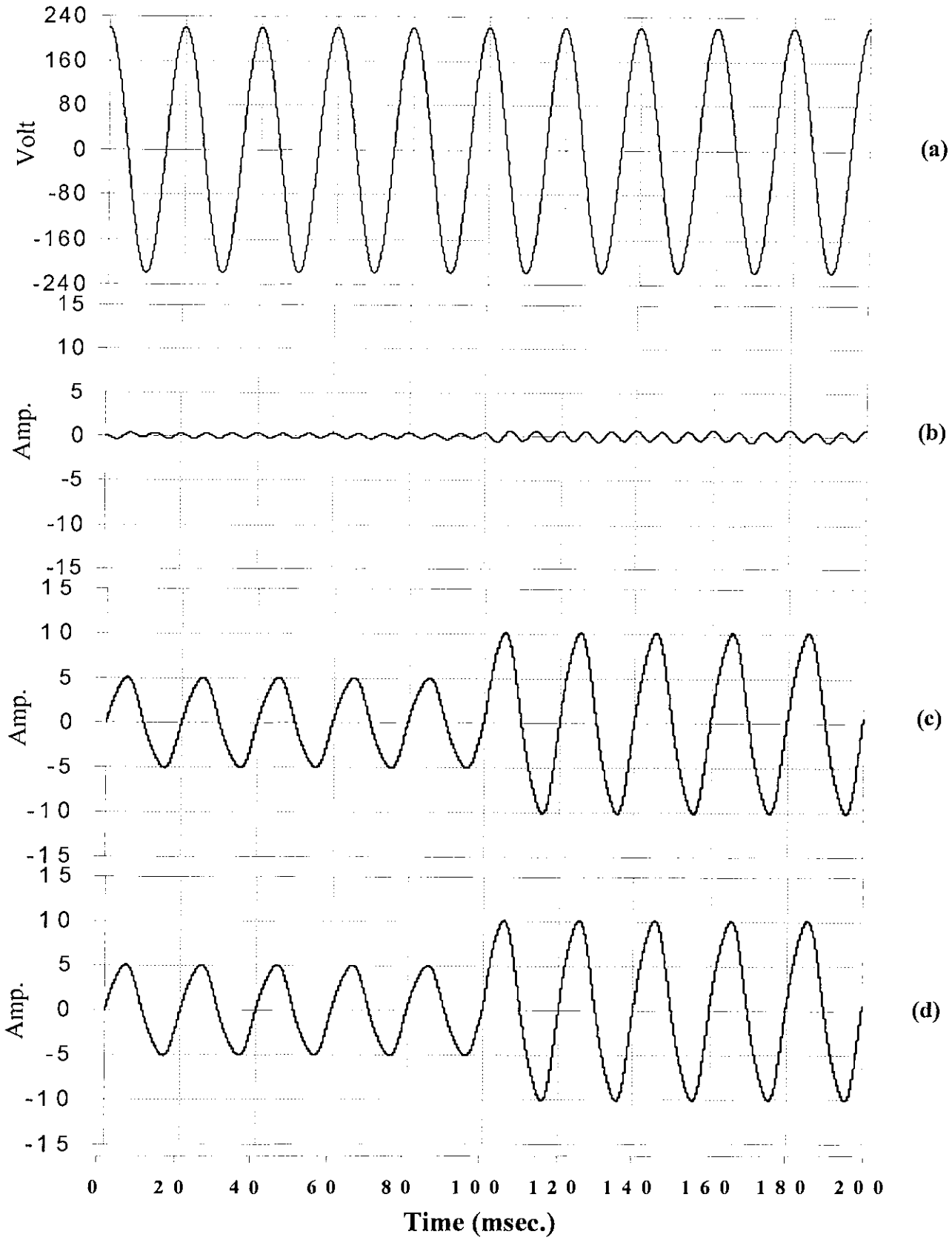


Fig.(3-11): Simulation results for θ=90° lag, f_s= 50 Hz. (a) Mains voltage $v_s(t)$, (b) Estimated current $i_a(t)$, (c) Load current $i_l(t)$, (d) Reference current $i_{rh}(t)$.

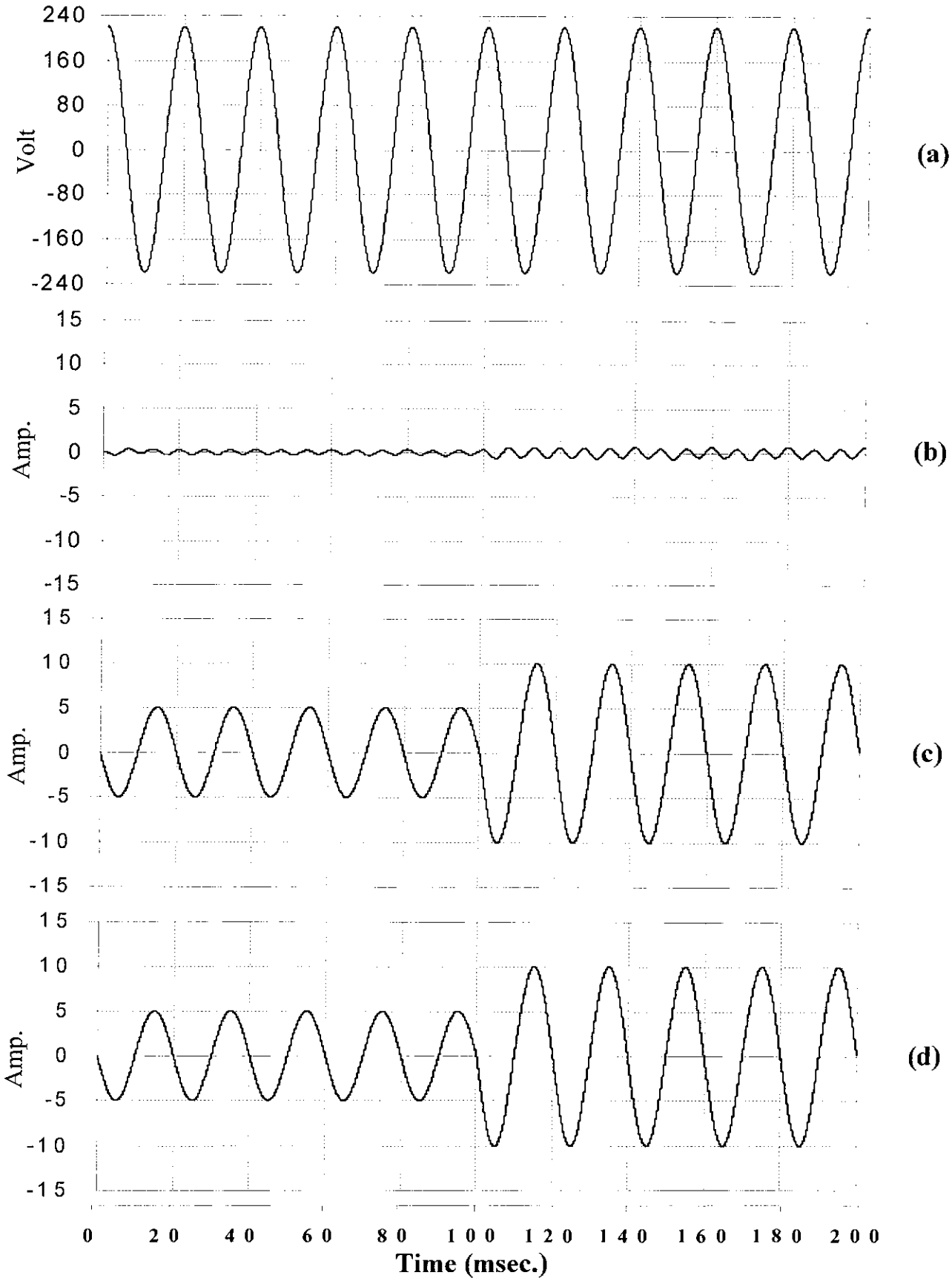


Fig.(3-12):Simulation results for $\theta=90^{o}$ lead, f_s= 50 Hz. (a) Mains voltage $v_s(t)$, (b) Estimated current $i_a(t)$, (c) Load current $i_l(t)$, (d) Reference current $i_{rh}(t)$.

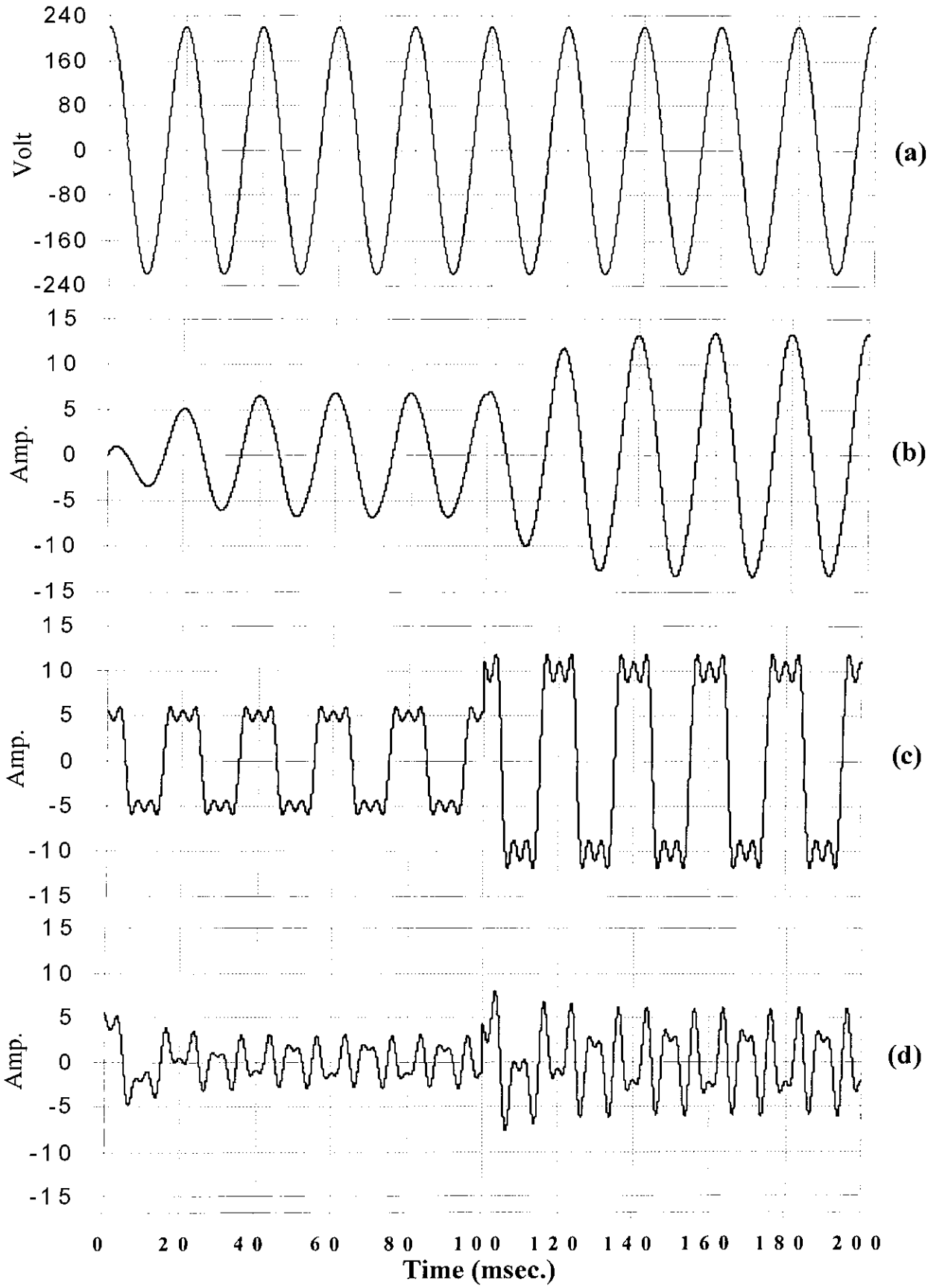


Fig.(3-13): Simulation results at rectifier load, f_s=50 Hz. (a) Mains voltage $v_s(t)$, (b) Estimated current $i_a(t)$, (c) Load current $i_l(t)$, (d) Reference current $i_{rh}(t)$.

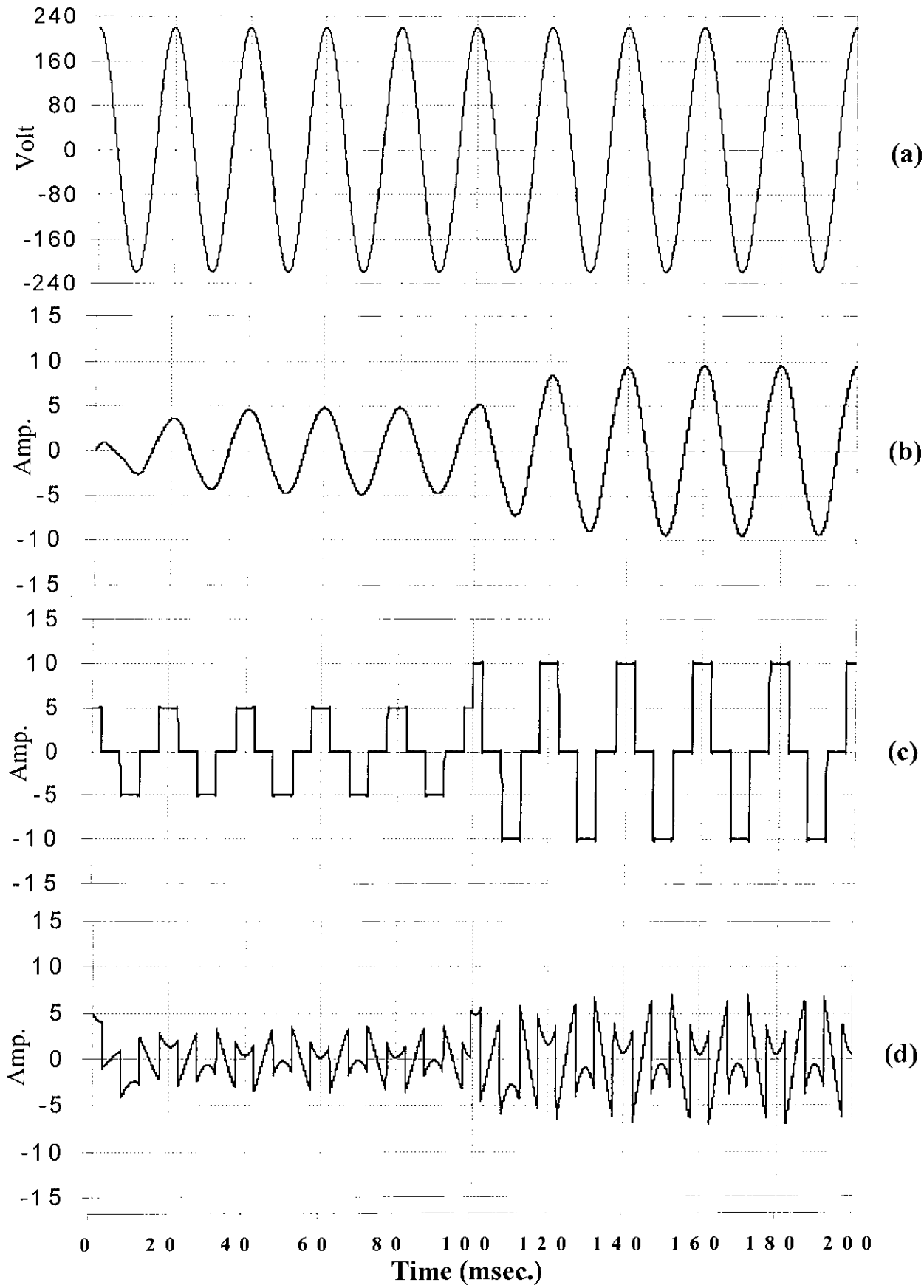


Fig.(3-14):Simulation results with rectifier load, R - C at dc side, f_s=50 Hz. (a) Mains voltage $v_s(t)$, (b) Estimated current $i_a(t)$, (c) Load current $i_l(t)$, (d) Reference current $i_{rh}(t)$.

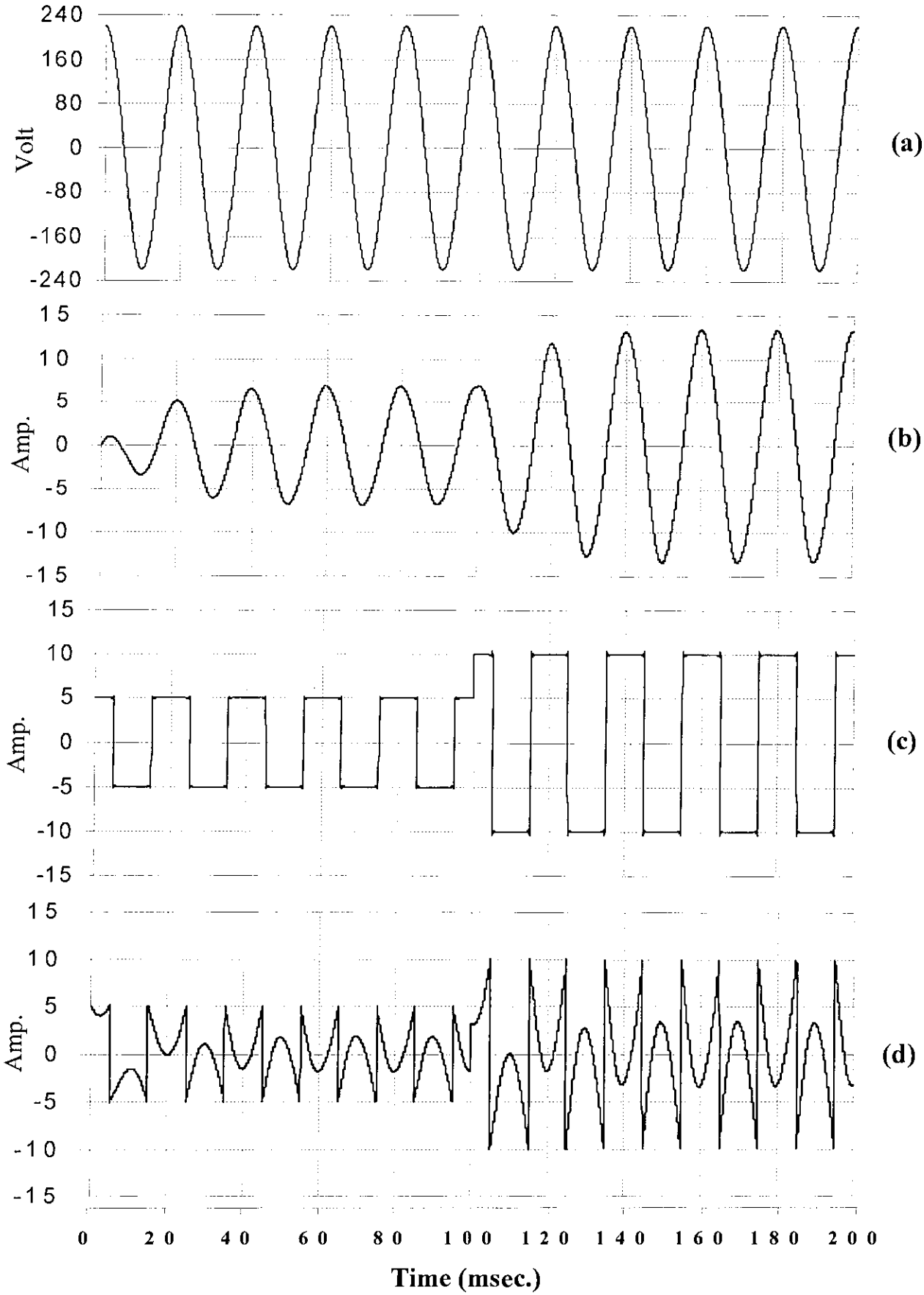


Fig.(3-15):Simulation results with rectifier load, R - L at dc side, f_s=50 Hz. (a) Mains voltage $v_s(t)$, (b) Estimated current $i_a(t)$, (c) Load current $i_l(t)$, (d) Reference current $i_{rh}(t)$.

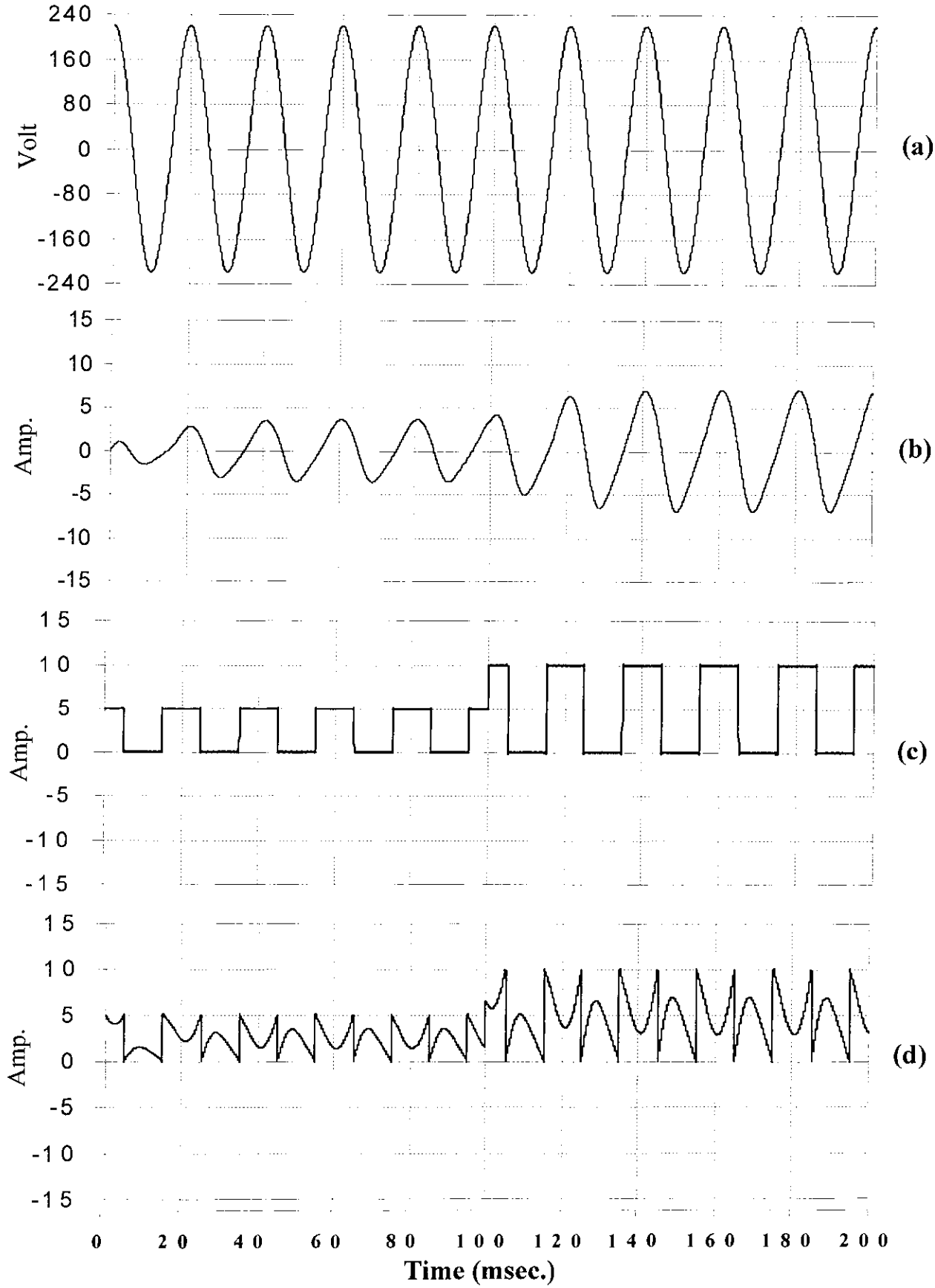


Fig.(3-16): Simulation results with half wave rectifier load, f_s= 50 Hz. (a) Mains voltage $v_s(t)$, (b) Estimated current $i_a(t)$, (c) Load current $i_l(t)$, (d) Reference current $i_{rh}(t)$.

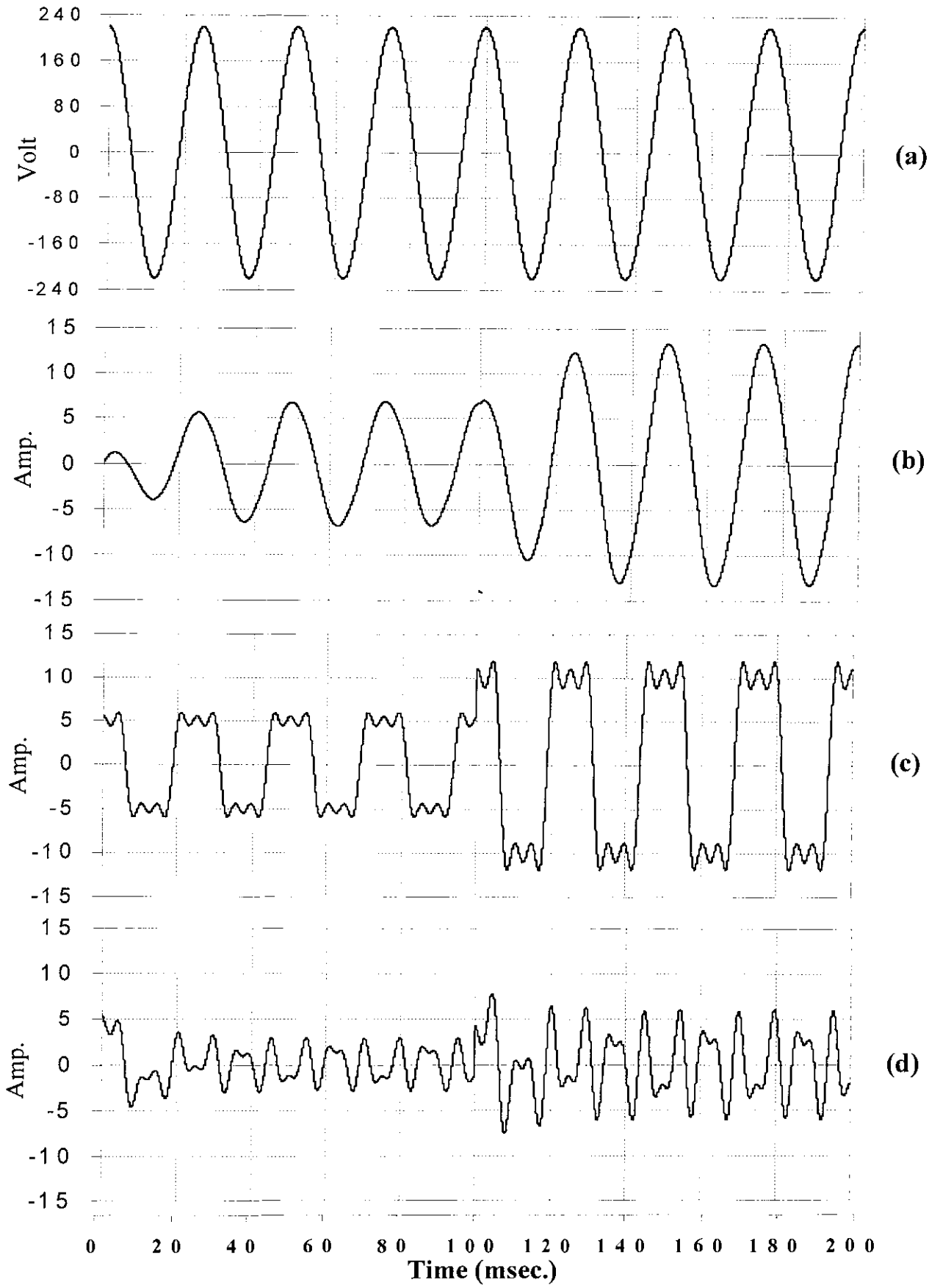


Fig.(3-17): Simulation results for rectifier load, f_s=40 Hz. (a) Mains voltage $v_s(t)$, (b) Estimated current $i_a(t)$, (c) Load current $i_l(t)$, (d) Reference current $i_{rh}(t)$

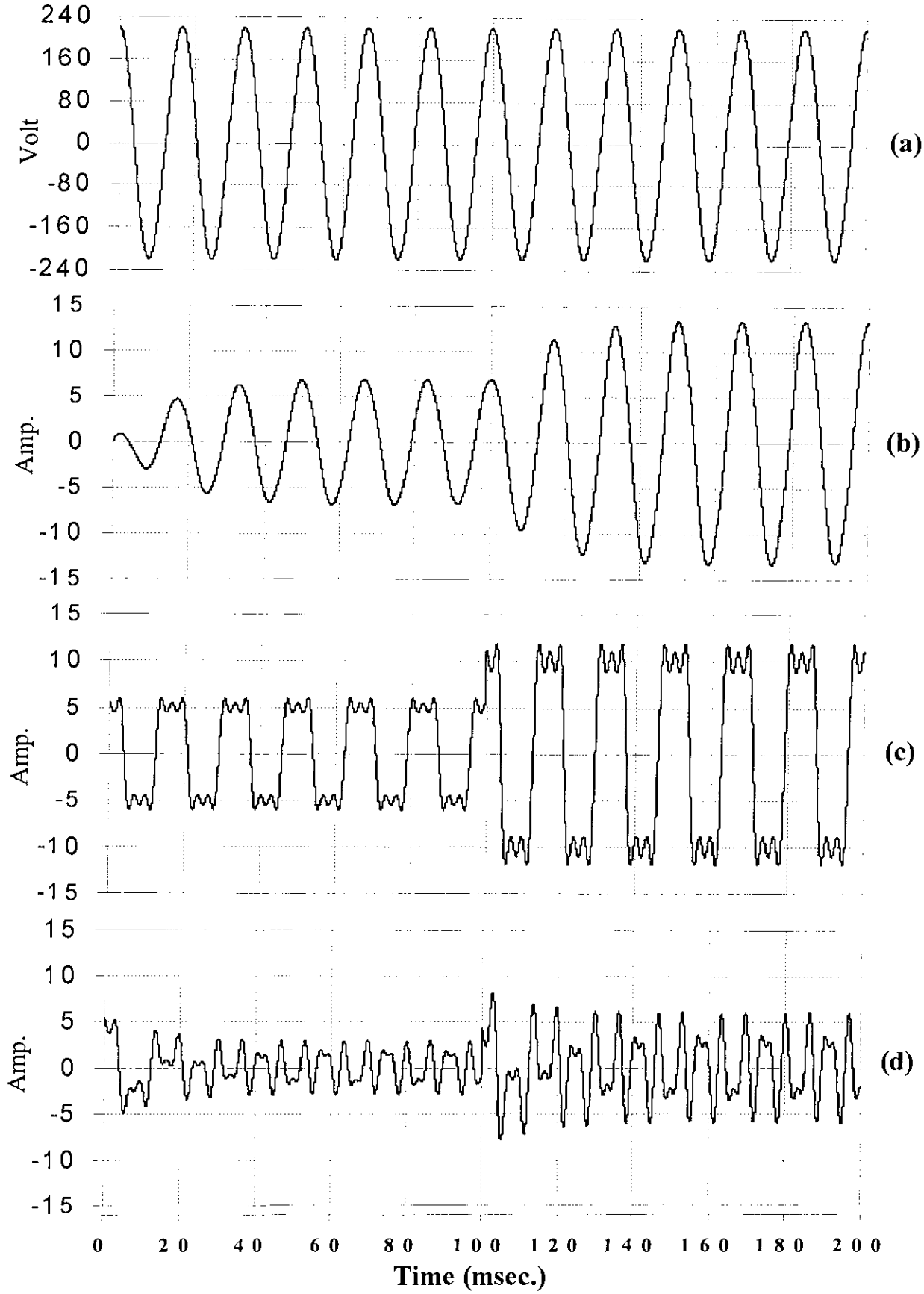


Fig.(3-18): Simulation results for rectifier load, f_s=60 Hz. (a) Mains voltage $v_s(t)$, (b) Estimated current $i_a(t)$, (c) Load current $i_l(t)$, (d) Reference current $i_{rh}(t)$

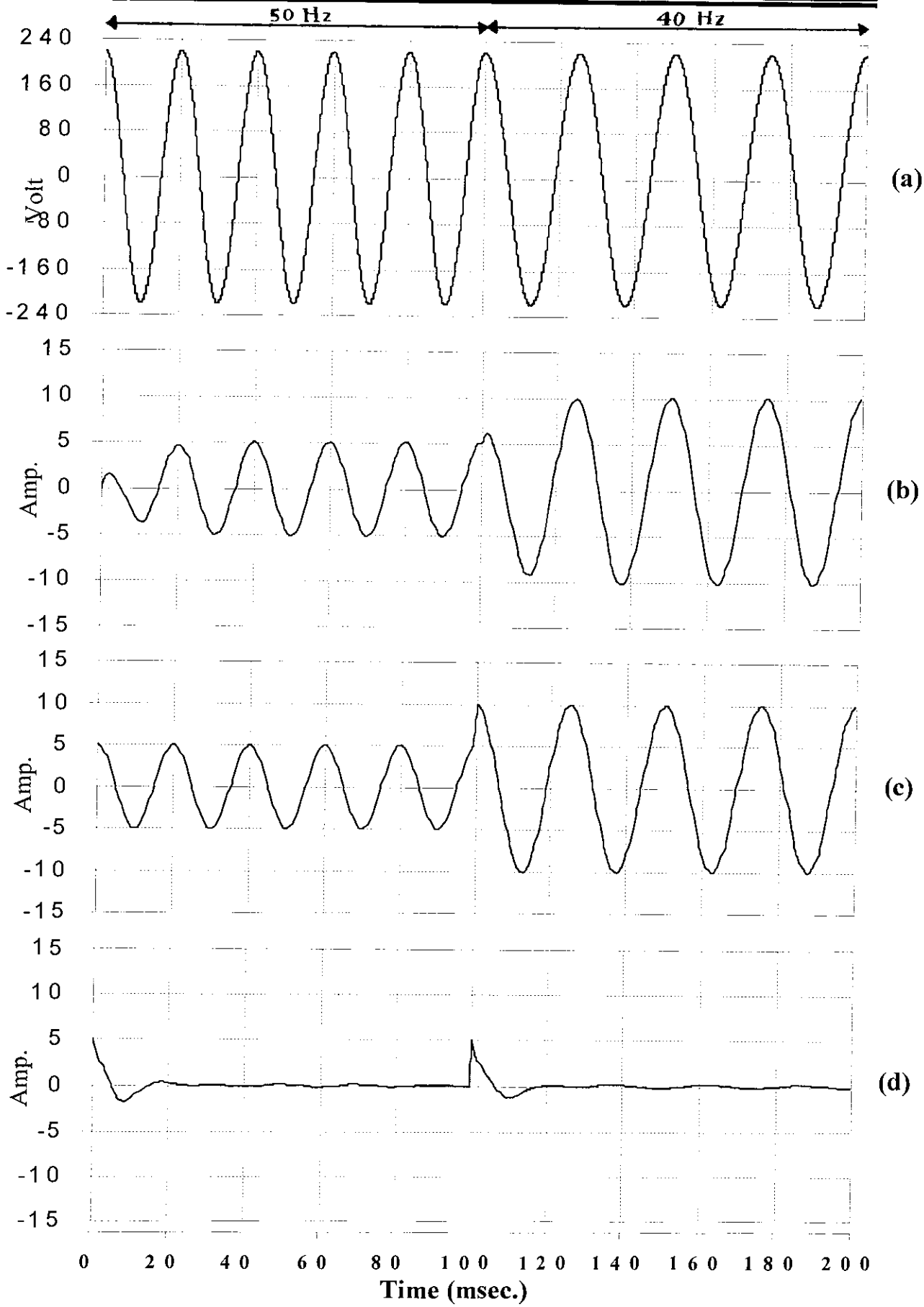


Fig.(3-19): Simulation results for $\theta = 0^{\circ}$. (a) Mains voltage $v_s(t)$, (b) Estimated current $i_a(t)$, (c) Load current $i_l(t)$, (d) Reference current $i_{rh}(t)$.

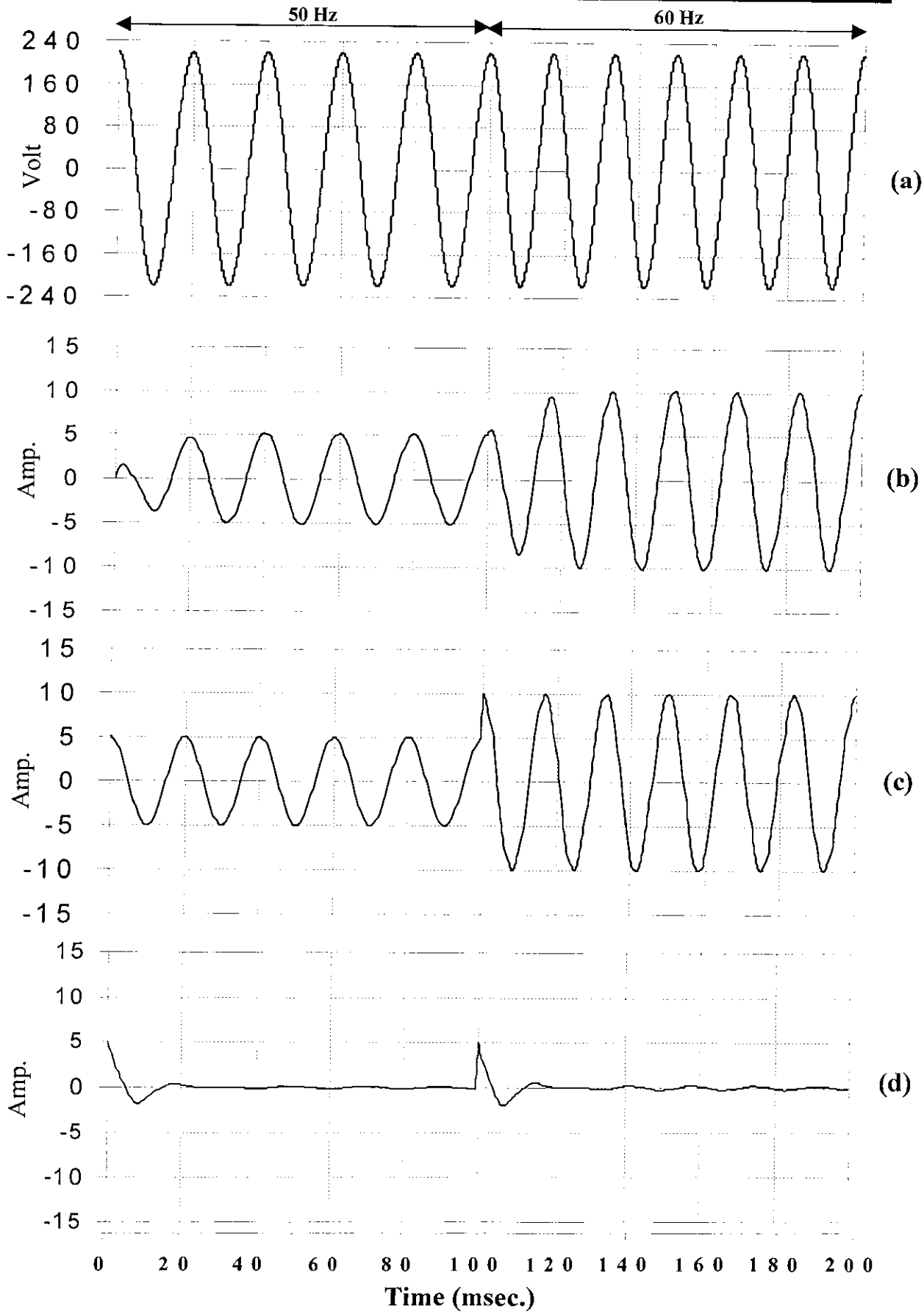


Fig.(3-20): Simulation results for $\theta = 0^{\circ}$. (a) Mains voltage v_s (t), (b) Estimated current i_a (t) , (c) Load current i_l (t), (d) Reference current i_{rh} (t).

CHAPTER FOUR

Experimental Realization and Investigations of the Designed Single and Three-Phase PWM-APFs

3.1 Introduction: -

The heart of the active power filter is the control circuit, not only because this circuit is one of the three main circuits to implement the APF compensation characteristics, but because it is responsible for generating the reference current where the innovation in the modern researches of the active power filter is presenting a novel control techniques to generate this current. These techniques have made remarkable progress in desirable technical features, such as fast response time and flexible of control coupled with commercial success due to their acceptable cost.

The conventional control methods of the active power filter used to obtain the required reference current are based on electronic filters or instantaneous power theory. Electronic filters, usually of the band pass filter type, have the drawback that a small change in the mains frequency may cause significant phase shift at the output. Therefore, to overcome this problem, the precision components and frequency adjusting have been used, but this would be valid only for the operating frequency and would not compensate the change due to component aging and temperature. On the other hand, the instantaneous power theory usually needs four to six high precision analogue multipliers and dividers per phase to implement the transformations. Thereby, this circuit becomes complex and sensitive to component parameter variations [4][17-19].

In this work, a new control strategy for single and three – phase active power filter is presented and analyzed. This is quite different in principle from the conventional control strategy, thus giving better compensation characteristics. The proposed method presents the following advantages:

1- The presented technique is simple than the instantaneous power theory – based design because this method has only two multipliers per phase and only one current sensor.

power circuit. A generation and amplification of the pulses are implemented by the drive circuit.

The drive circuit needs to be isolated. Two methods are suggested to accomplish this task; pulse transformer and optoisolator. The pules transformer has the drawbacks of larger size and the need to another component (as monostable **74121**) to convert a positive or negative edge to the specified width, therefore, the optoisolator has been used in this work.

The main and auxiliary transistors in the designed circuit are of **MOSFET** type, because this type of the transistors has the advantages of requiring only small input current and having high switching speed [37].

The next sections of this chapter will be devoted to the construction, operation and investigation of the individual parts of the compensating system.

4.2.1 The control circuit: -

Figure (3-1) shows the control circuit of the implemented APF that includes two major generating circuits; reference sinusoid generating circuit and active current estimation circuit. Two signals are fed to the proposed control circuit; the first is the measured load current $i_l(t)$ and the other signal is the sensed practical mains voltage $v_s(t)$.

4.2.1.1 In-phase sinusoid generator: -

Figure (4-1) shows the implemented electronic circuit for generating unity sinusoidal cos(ωt) in- phase with the mains voltage. The phase-locked loop (PLL) circuit is used to generate the synchronized pulses with mains voltage and exact phase tracking in a wide range of frequencies (see appendix A [38]). Then, these pulses are integrated and converted to triangular

waveform. Finally, the output sinusoidal signal is generated from the triangular wave by nonlinear circuit and R-C low pass filter [39], also, the noninverting op-amp in this figure used to adjust unity gain, and the capacitor (C_3) employed to remove dc offset of the integral circuit.

4.2.1.2 Active current estimator: -

As shown in Fig.(3-1) this circuit consists of two multipliers, low pass filter and P-I controller (dashed block diagram). Implementation of these circuits will be illustrated in the following sections:

a) Analogue multiplier

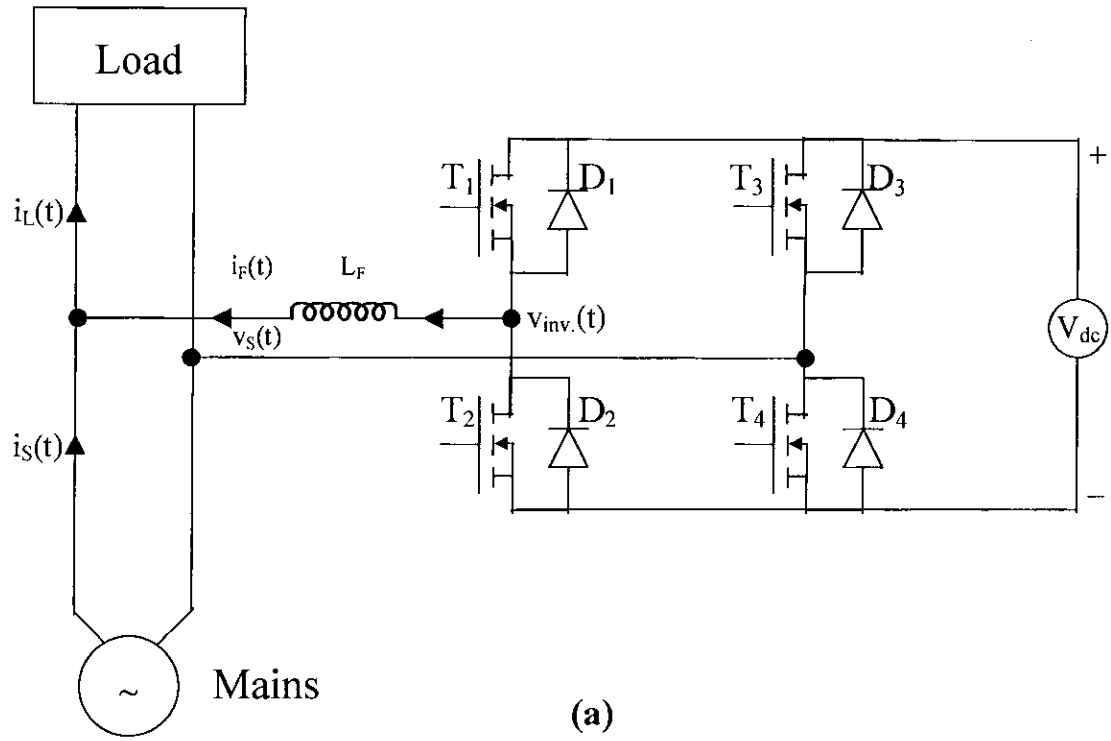
The integrated circuit **1495** is employed as a multiplier. The configuration of this integrated circuit is shown in Fig.(4-2). Two multipliers are used per phase; the first multiplies the references current by cos(ωt) and the second multiplies the estimated magnitude of the active current by cos(ωt) too.

b) Low pass filter

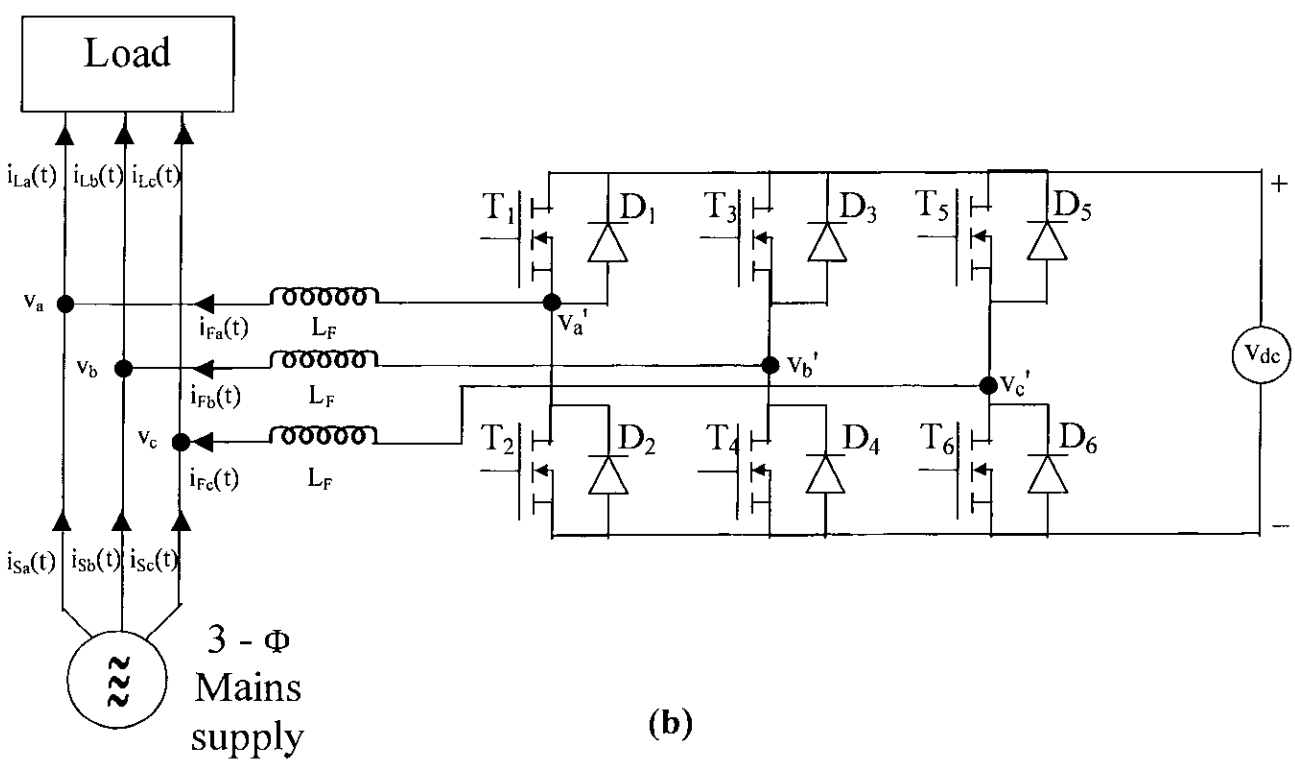
The design of the low pass filter is the most important in the control circuit, because various compensation characteristics are obtained in accordance with the cut-off frequency and order of the low-pass filter. Therefore, the implemented LPF in this work has a cut-off frequency of **10Hz**, which is below the frequency of the mains to obtain only the dc component that represents the magnitude of the active current. The components of this filter are selected as shown in appendix B.

c) P-I controller

This controller consists of two parts; proportional part and integral part. As it has been shown in section (3.5.1), the parameters of this controller



(a)



(b)

Fig. (2 – 4): Voltage source inverter
(a) Single phase system
(b) Three-phase system

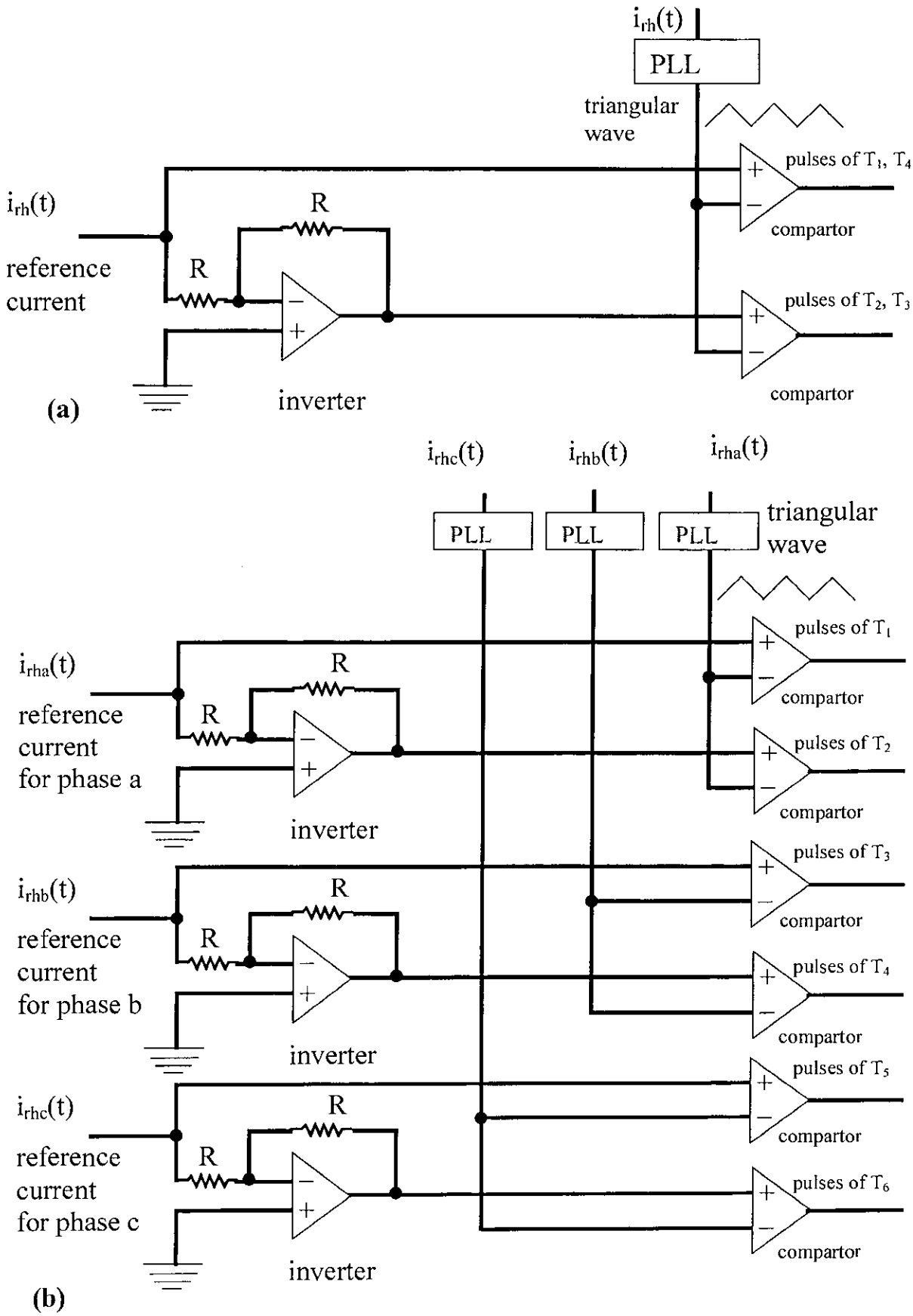


Fig.(4–3):The pulses generation part of the drive circuit.
(a) Single phase system.
(b) Three phase system.

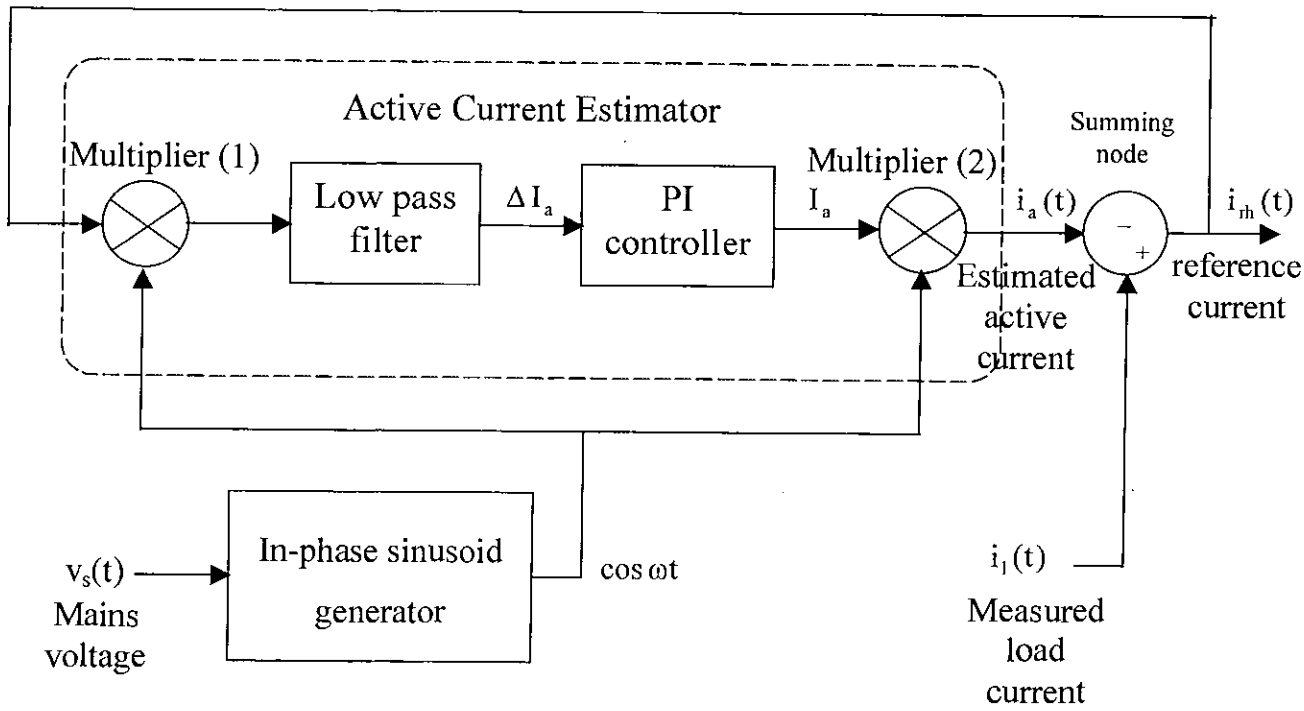
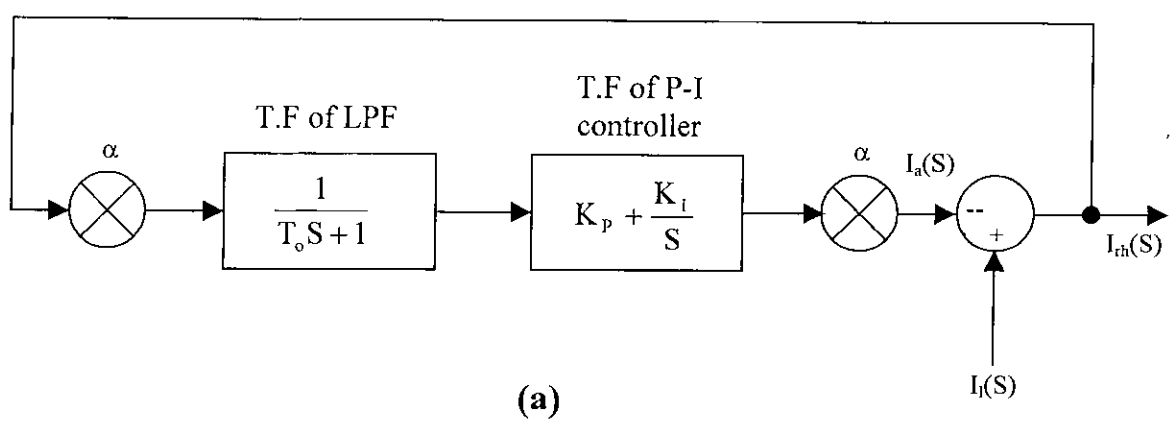
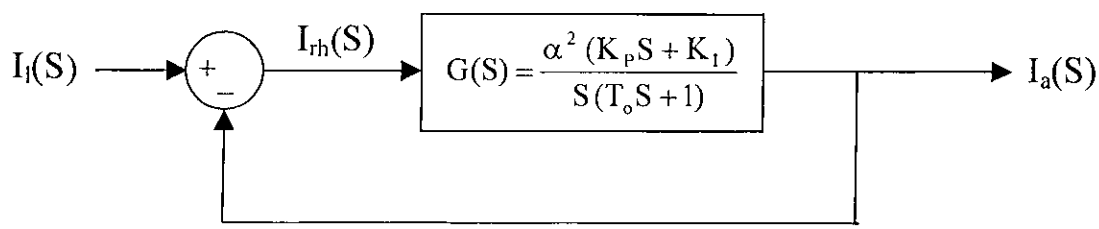


Fig.(3-1): Block diagram of the control circuit for APF (one phase).



(a)



(b)

Fig.(3-2): (a) and (b) closed loop of the control circuit in a s-domain (one phase).

Selection of the LPF elements

The transfer function of the first order LPF, shown in Fig. B-1, is:

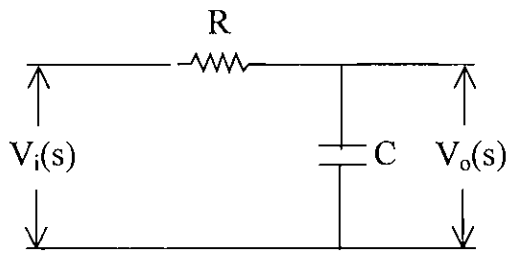


Fig. (B-1): First order LPF.

$$\frac{V_i(s)}{V_o(s)} = \frac{1/RC}{S + 1/RC}$$

$$= \frac{\omega_o}{S + \omega_o} \qquad \text{---------- (B-1)}$$

where $\omega_o = \frac{1}{RC}$ is the cut-off frequency of the filter.

choosing $\omega_o = 20\pi$ rad/Sec. yields

for $R = 1.5\,K\Omega$.

$C = 10\ \mu F$.

Table 4-2:Capacitive load test.

MAINS		LOAD	
Phase angle (deg.)	Power factor (cosϕ)	Phase angle (deg.)	Power factor (cosϕ)
0	1.000	0	1.000
2.5	0.999	10	0.984
2.5	0.999	20	0.939
2.5	0.999	30	0.866
3	0.998	40	0.766
3	0.998	50	0.642
4	0.997	60	0.500
6	0.994	70	0.342

The above results are plotted as in Fig.(4-18b). It is clear that the phase angle between mains voltage and current is very small (between 2.5 and 6 degrees) for different values of load phase angle.

Figure (4-19b) illustrates the experimental waveform of load voltage, load current, mains voltage and mains current.

c) The harmonic cancellation

The second objective of the active power filter has been verified with the bridge rectifier used a nonlinear load. The result is that the mains current has been made sinusoidal wave and the mains power factor has become unity.

Figures (4-20a and 4-20b) show the load voltage, load current, mains voltage and mains current for two cases; the first when the dc load of the bridge rectifier has inductive filtering and the second when the output filter is a capacitive.

Table 4-1: Inductive load test

MAINS		LOAD	
Phase angle (deg.)	Power factor (cosϕ)	Phase angle (deg.)	Power factor (cosϕ)
0	1.000	0	1.000
2	0.999	10	0.984
2.5	0.999	20	0.939
3.5	0.998	30	0.866
3.5	0.998	40	0.766
5	0.996	50	0.642
5	0.996	60	0.500
7	0.992	70	0.342

The above results are plotted as in Fig.(4-18a). It is clear that the power factor at the mains voltage and current is near unity for different values of load power factor.

The practical waveform of load voltage, load current, mains voltage and mains current are as in the Fig.(4-19a).

b) Capacitive load test

The results of the compensation for a capacitive load with different values of power factor are summarized in table 4-2. These results also, confirm the effectiveness of the filter in compensating the capacitive reactive power.

Figure (4-10) illustrates another ability of the designed control circuit, where it can be operating at frequencies ranging from **40Hz** to **60Hz** covering the major frequencies **50Hz** and **60Hz**.

4.3.3 The drive circuit:-

The output signal of the control circuit $i_{rh}(t)$ is fed to the drive circuit that in turn compares this signal with a synchronized generated triangular waveform to produced the modulated pulses which are fed to the corresponding switches after amplification. The drive circuit configuration is shown in Fig.(4-5), whereas its output with the corresponding modulating current are shown in Fig.(4-11) for different types of loads; Fig.(4-11a) corresponding to a linear inductive load whereas Figs.(4-11b and 4-11c) show the reference signal and modulated pulses for two types of nonlinear loads. These figures show that the drive circuit will produce driving pulses which are width modulated corresponding to reference signal $i_{rh}(t)$, as it is required to cancel the reactive and harmonic components of the main current.

4.3.4 The power circuit:-

The MOSFET power transistors of the power circuit are driven by the pulse-width modulated pulses that are generated by the drive circuit. These pulses and their sequence in driving the transistors are shown in Fig.(4-12) for single-phase power circuit.

The compensating current and output voltage waveforms of the designed active power filter are produced in accordance to the driving pulses as illustrated in Fig.(4-13) for linear loads (inductive or capacitive load) and nonlinear load (full wave rectifier with RL series at dc side).

these tests are a sinusoidal output waveform that is in- phase with the input signal as illustrated in Figs.(4-6 and 4-7). These figures confirm that the implemented phase-locked loop circuit will produce the desired in-phase sinusoidal waveform even if then supply voltage (input waveform) is highly distorted.

4.3.2 The control circuit: -

The designed control circuit that is used to estimate the active component and the modulating reference component of the load current has been subjected to the following tests:

a) Linear load test

Inductive and capacitive linear loads with different power factors have been connected to the supply and the control signals (load current and supply voltage) are fed to the control circuit. The results of this test that are shown in Fig.(4-8) confirm its excellent predicted performance for all considered test cases. It can be noticed that modulating signal with zero amplitude is generated for the case of unity power factor as shown in Fig.(4-8a), whereas a pure sinusoidal reactive modulating signal is generated for the case of zero power factor as shown in Figs.(4-8c and 4-8e).

b) Non-linear load test

Another salient point is clarified in Figs.(4-9a, 4-9b and 4-9c) where the control circuit has been tested for three types of the nonlinear loads. These results prove the capability of the active power filter in the harmonics cancellation. The reference current in these cases represents the harmonic components in the load current.

(proportional parameter and integral parameter) have large effects on the response of the control circuits. Optimal response of the system (i.e., fast and accurate response) is obtained with $\mathbf{K_P=35}$ and $\mathbf{K_I=400}$. Therefore, this type of controller is preferred over an integral controller and it offers more flexibility to improve the performance of a system being compensating. Appendix C shows the implemented electronic circuits of the P-I controller.

4.2.2 The drive circuit:-

This circuit is responsible for generation and amplification of the pulse-width modulated signals. Figure (4-3) illustrates the circuits that generate the driving pulses for the single and three-phase active power filter. In these circuits, the reference (modulating) signal is compared with high frequency **(3kHz)** triangular waveform to generate pulses that are modulated according to the reference signal. Then, these pulses are amplified and fed to the transistors in the power circuit.

A phased-locked loop circuit has been used to generate two types of the signals (triangular waveforms and pulses). These signals synchronize with reference signal $i_{rh}(t)$ and has high frequency as shown in Fig.(4-4). Also in the same figure, the integrated circuits (**7490** and **7492**) operate as frequency divider to convert frequency of the pulses from **3kHz** to **50Hz** (input frequency).

Optical isolator has been used to isolate the control circuit from the high power side of the active power filter (see appendix D)[40]. Then, the modulated weak output signal of the isolator is amplified and fed to the corresponding transistor in the power circuit as shown in Fig.(4-5).

The output currents of the considered APF are shared between the transistors and diodes of the power circuit in a manner that maintains a continuity of the load current, i.e., when the transistors pair is off the parallel diodes of the second pair will be on as illustrated by Fig.(4-14).

4.3.5 Three- phase active power filter: -

The essential parts of the three - phase active power filter are the three-phase corresponding of the single phase APF parts as illustrated in Fig.(4-15).

The three-phase control circuit has been implemented to estimate the three-phase reference currents that are used to generate the driving pulses. The three-phase reference currents and the corresponding driving pulses are shown in Figs.(4-16 and 4-17) respectively.

4.3.6 Investigation of the APF characteristics:-

To verify the characteristics and performance of the designed active power filter, a prototype system has been constructed and tested. Several tests have been implemented in order to confirm the effectiveness of the active power filter. These tests include:

a) Inductive load test

The active power filter has been used to compensate the reactive power for different lagging load power factor and the results of such compensation are summarized in table 4-1, these results show that approximately unity power factor at the mains can be obtained using the designed APF.

4.2.3 The power circuit:-

This circuit is a voltage source inverter that operates in a current-controlled mode. The single and three-phase configurations of such circuit are shown in Fig.(2-4). The implemented active power filter have power circuits that consists of:

1- Moderate power transistors, (type **VN4000A**).

2- Moderate power diodes (type **BXY 71**).

3- DC voltage capacitor about **1500μF** on dc side.

4- Inductors on the ac side that have small values as **5mH**.

4.3 Experimental results: -

This section will illustrate experimentally the performance and characteristics of the different parts of the implemented active power filter system. Operation of these parts has been investigated by monitoring their response for the various testing conditions. These conditions include operation of the system; (i) with different types of loads (linear and nonlinear loads), (ii) with different load power factors (iii) with distorted and non-distorted supply voltage. Following are the investigations of the individual parts of the active power system:

4.3.1 In-phase sinusoid generating circuit:-

The output waveforms of the individual subcircuits that constituting the in-phase sinusoid genrating circuit are shown in Fig.(4-6). These waveforms are consistent with the predicted waveforms at the corresponding points of the circuit shown in Fig.(4-1).

The designed generating circuit has been tested for three different input waveforms (sinusoidal, triangular and rectangular waveforms). The results of

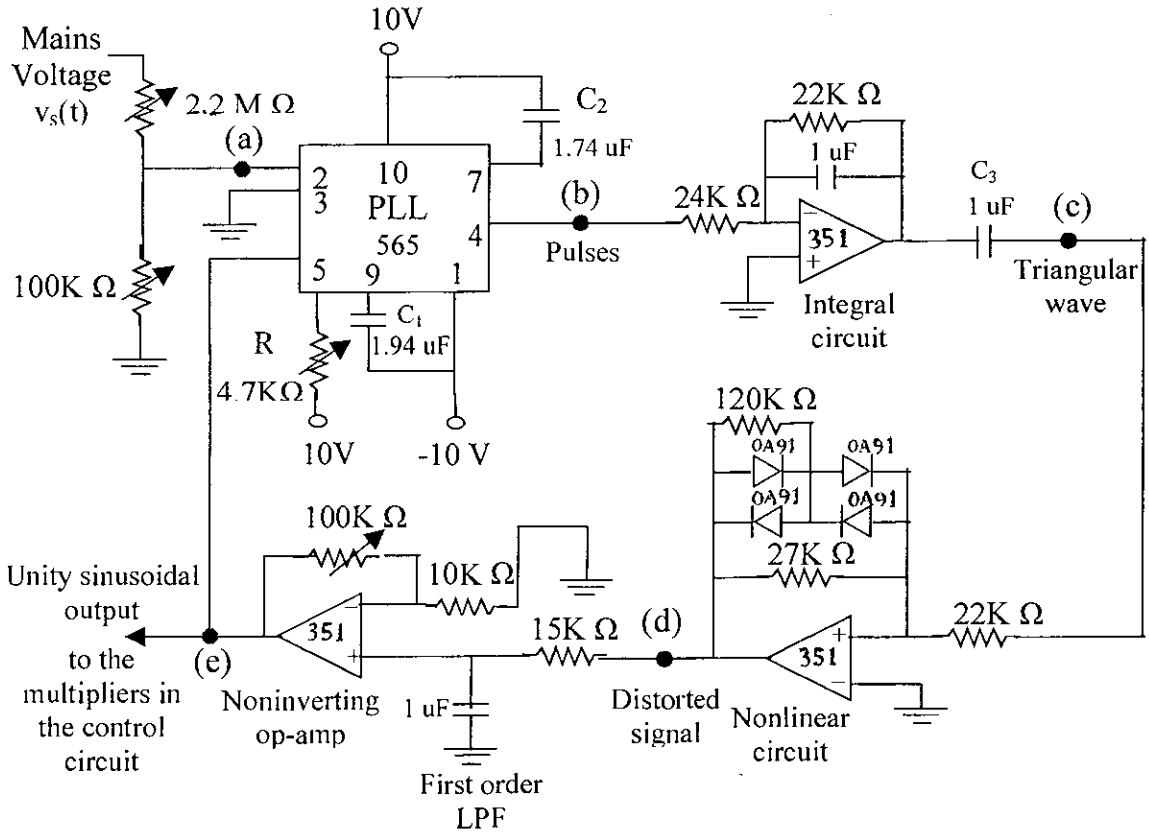


Fig.(4-1): Electronic circuit for generating unity sinusoidal in-phase with line voltage.

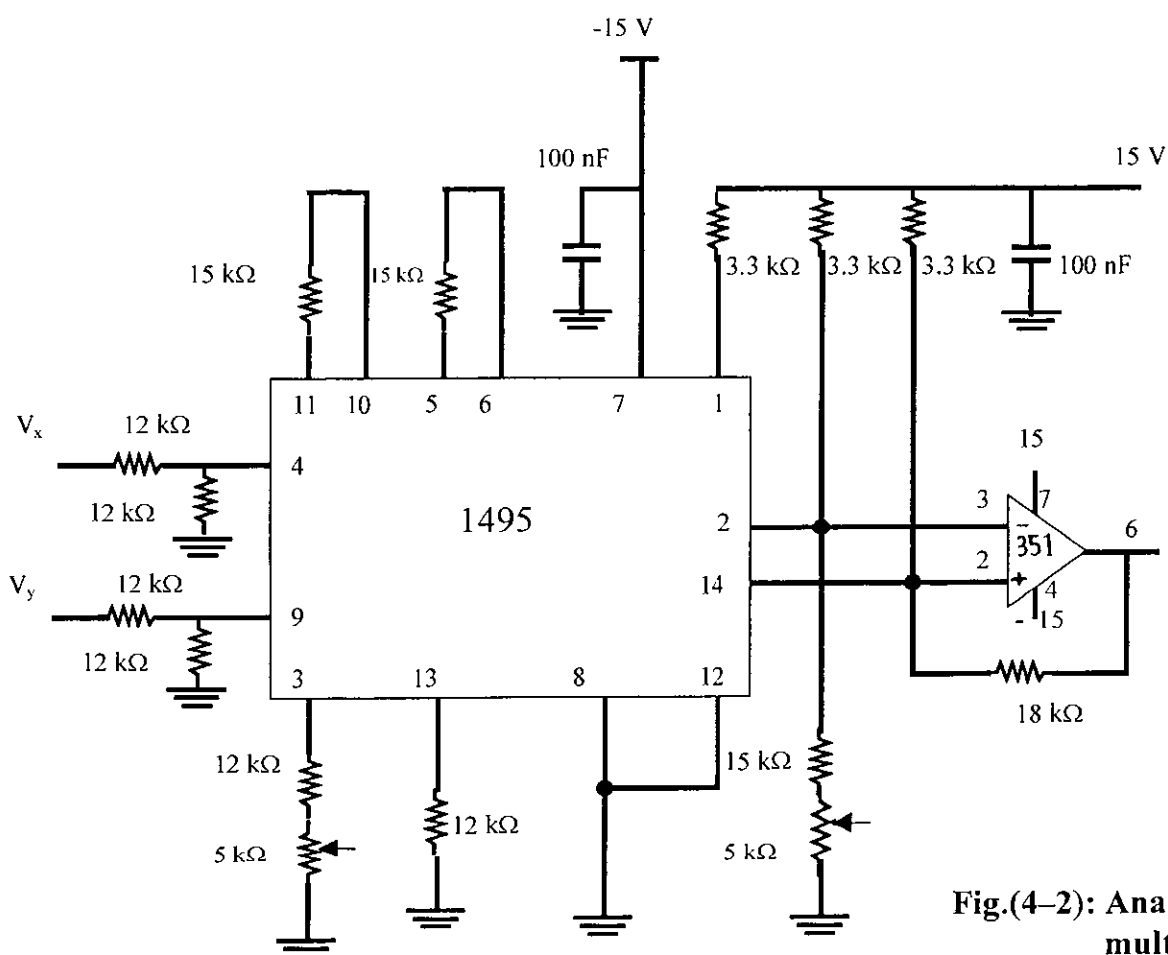


Fig.(4–2): Analogue multiplier.

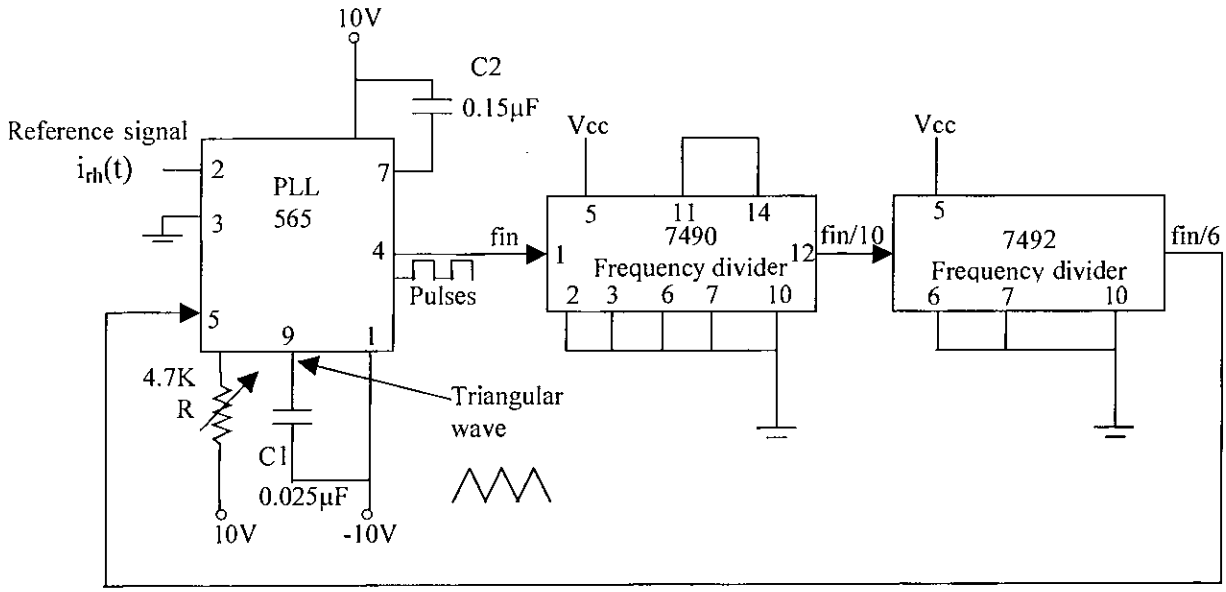


Fig.(4-4): The synchronization circuit between the reference current and triangular wave.

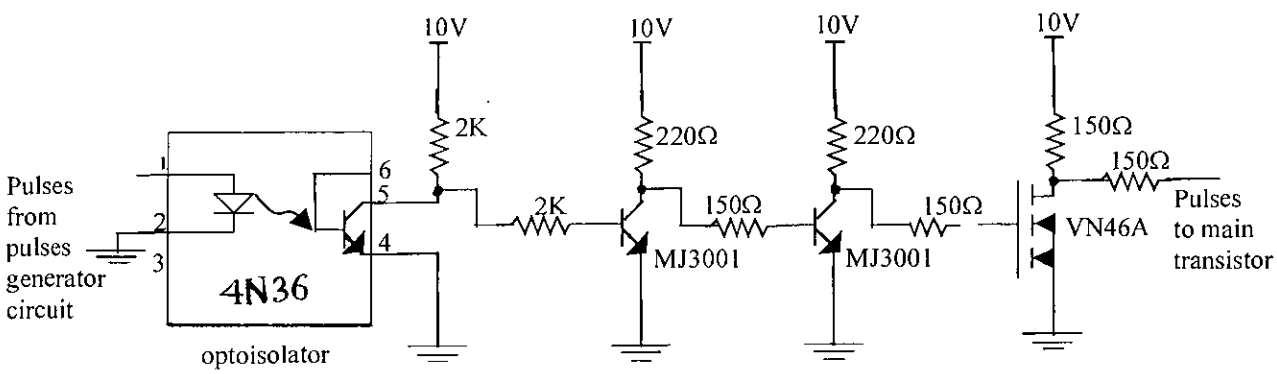
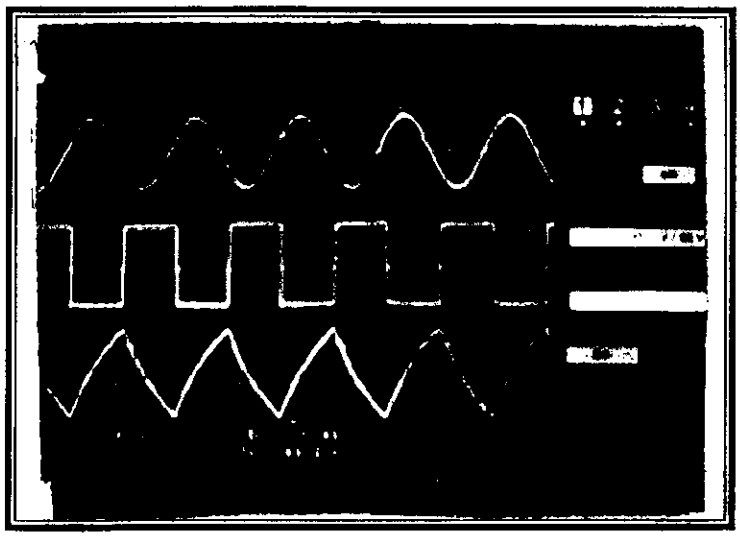


Fig.(4-5): The amplification part of the drive circuit.

(a) 1.5V/div.

(b) 5V/div.

(c) 5V/div.

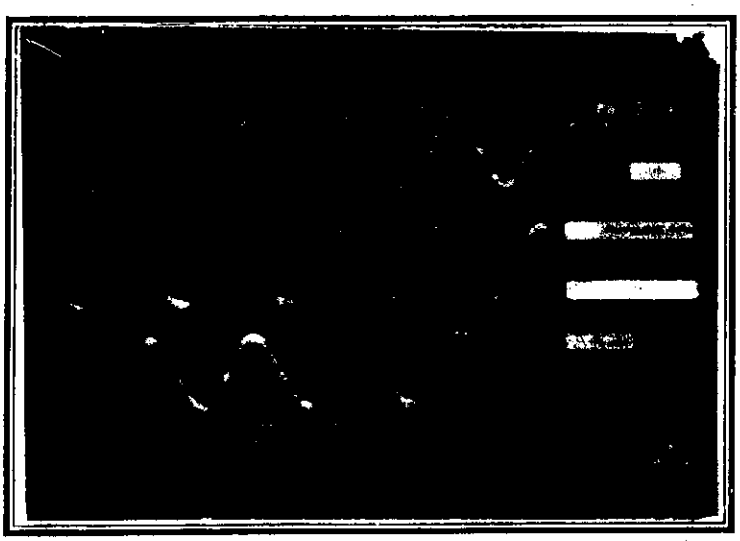


10 m sec/div.

(a) 1.5V/div.

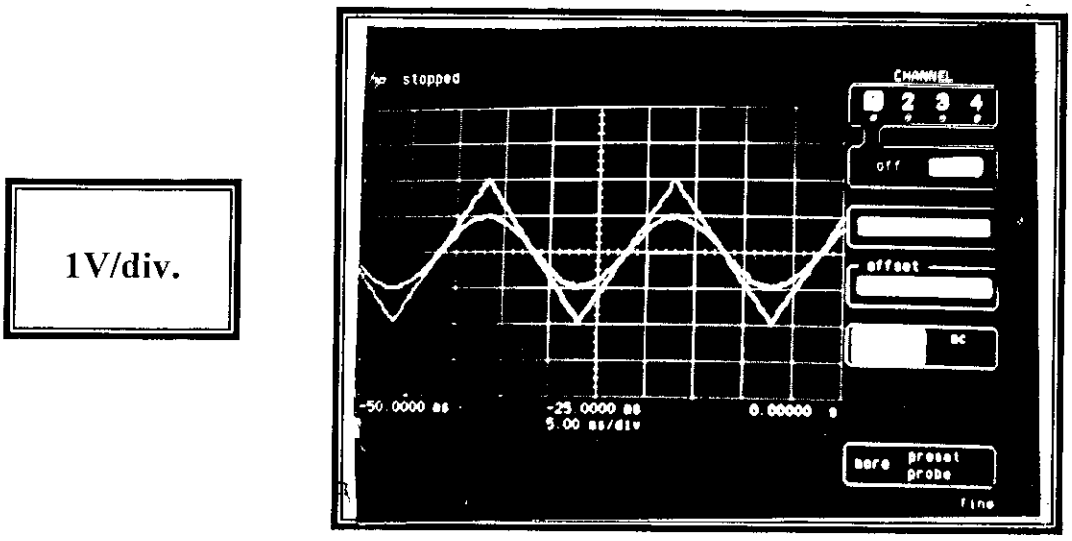
(d) 0.5V/div.

(e) 1V/div.

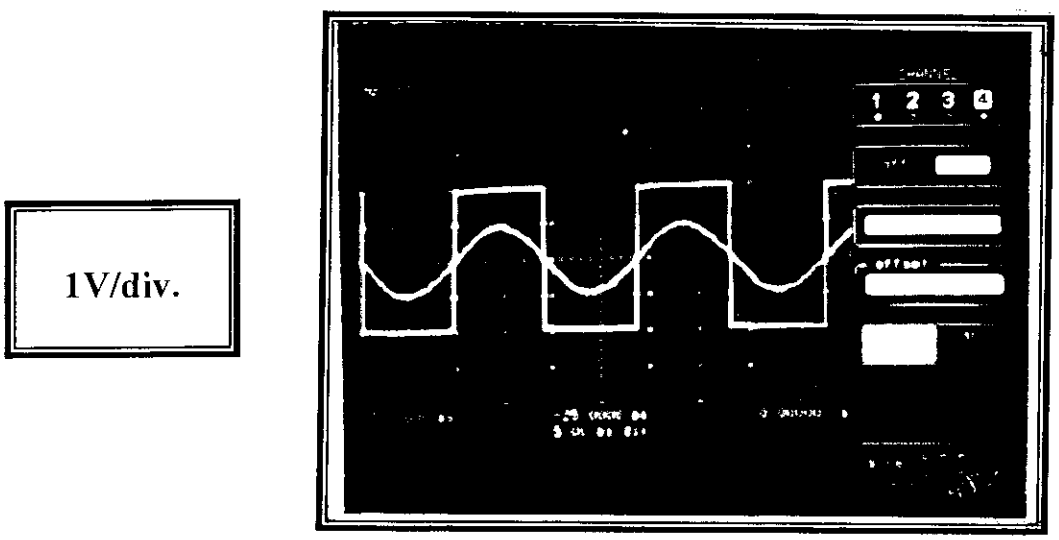


10 msec/div.

Fig.(4-6): In-phase sinusoid generating circuit operation. (a) Mains voltage $v_s(t)$, (b) Output of IC 565, (c) The output signal of the integral circuit, (d) The output signal of the nonlinear circuit, (e) In-phase sinusoid with mains voltage.



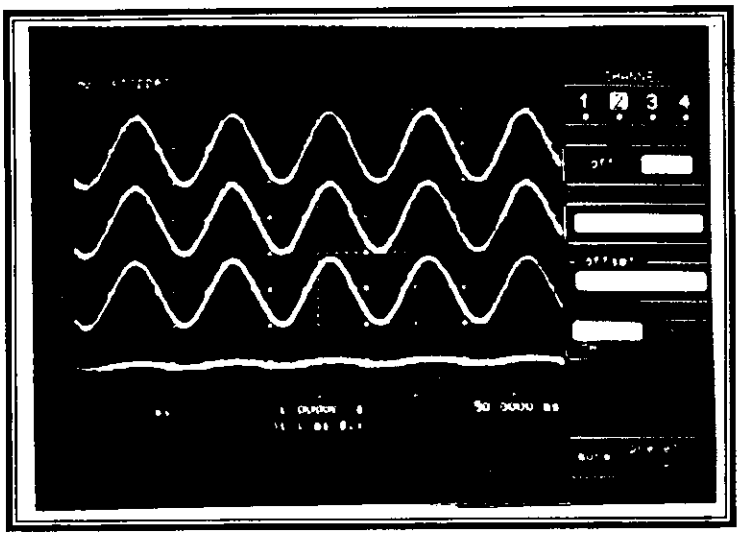
(a)



(b)

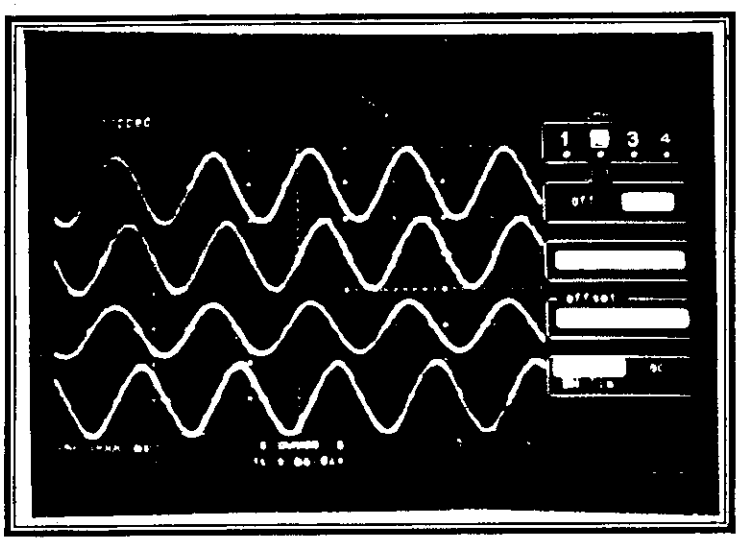
Fig.(4-7): (a) and (b) The triangular wave and square wave as an input signal of a PLL circuit respectively and the sinusoid wave is output signal. (5 msec./div.)

(1) 50V/div.
(2) 1.5A/div.
(3) 1.5A/div.
(4) 1.5A/div.



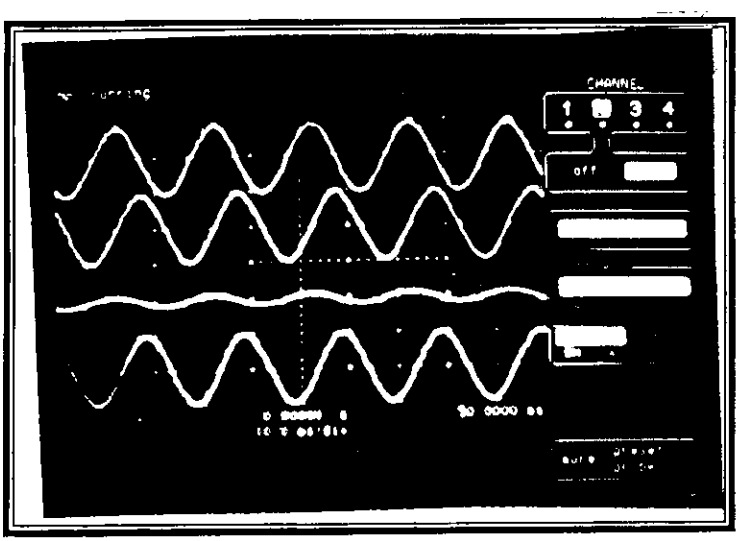
(a)

(1) 50V/div.
(2) 1.5A/div.
(1) 1.5A/div.
(2) 1.5A/div.



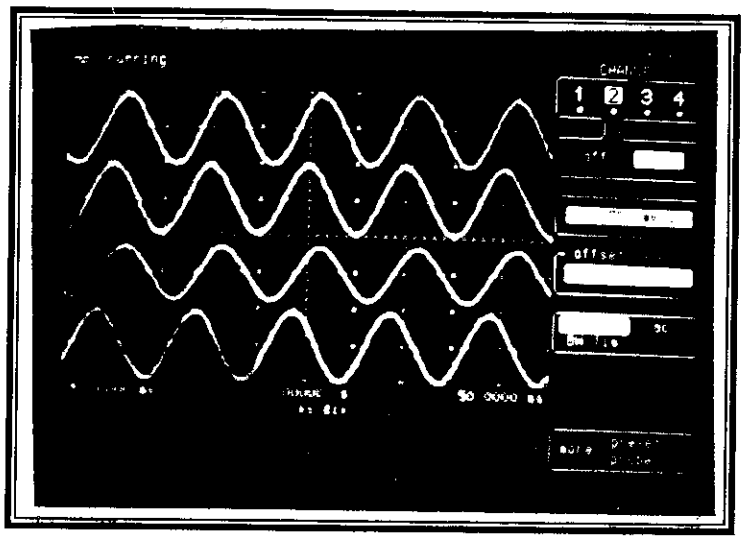
(b)

(1) 50V/div.
(2) 1.5A/div.
(3) 1.5A/div.
(4) 1.5A/div.



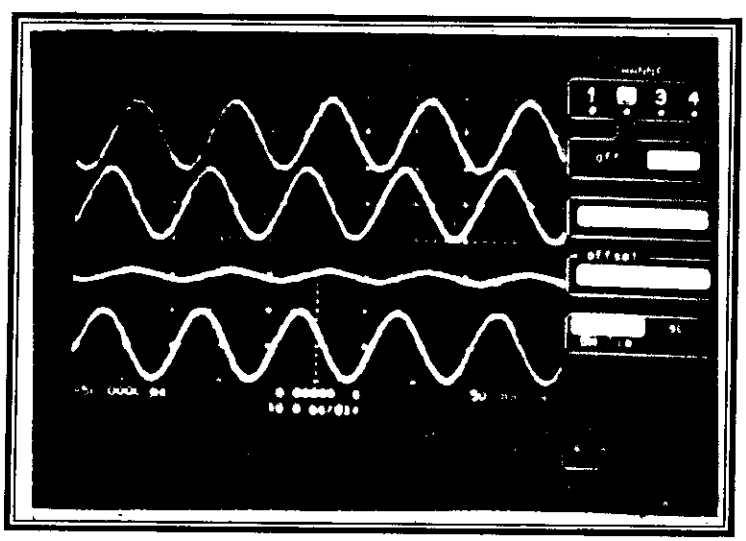
(c) (Cont.)

(1) 50V/div.
(2) 1.5A/div.
(3) 1.5A/div.
(4) 1.5A/div.



(d)

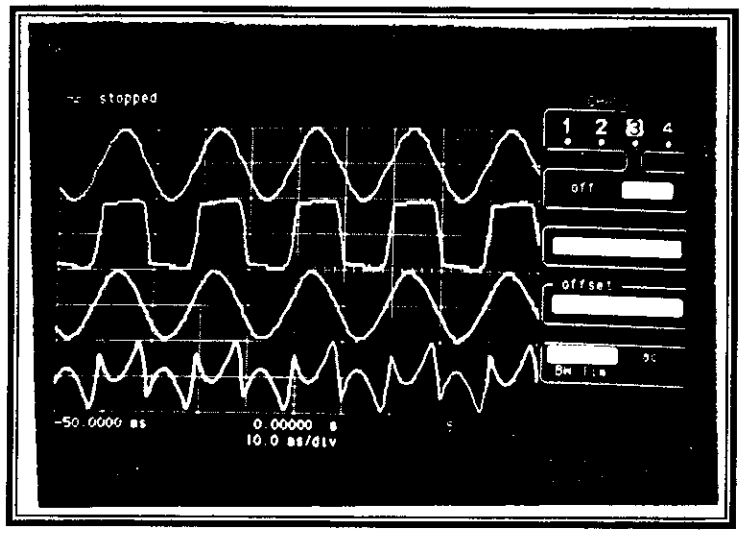
(1) 50V/div.
(2) 1.5A/div.
(3) 1.5A/div.
(4) 1.5A/div.



(e)

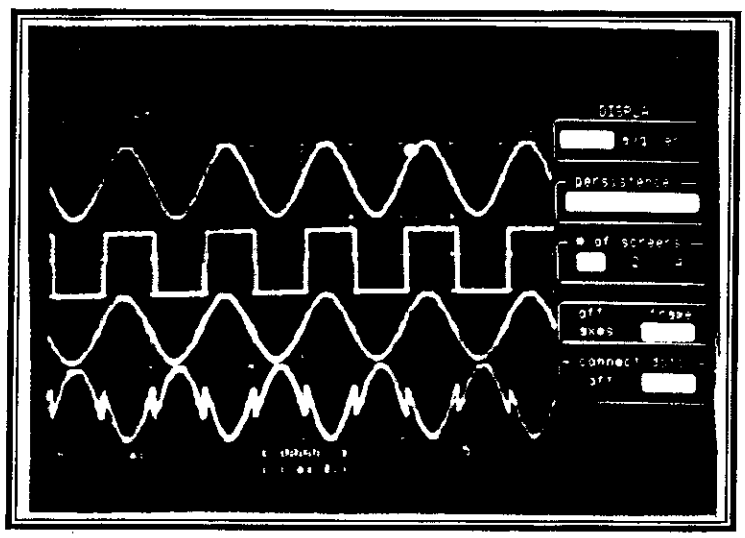
Fig.(4-8): Experimental results of the linear load test. (10 msec./div.)
(a) $\theta=0^{\circ}$, (b) $\theta=50^{\circ}$ lag., (c) $\theta=90^{\circ}$ lag.,(d) $\theta=50^{\circ}$ lead, (e) $\theta=90^{\circ}$ lead.
(1)Mains voltage $v_s(t)$, (2) Load current $i_l(t)$,
(3) Estimated current $i_a(t)$, (4) Reference current $i_{rh}(t)$.

$v_s(t)$ 50V/div.
$i_l(t)$ 1.5A/div.
$i_a(t)$ 1.5A/div.
$i_{rh}(t)$ 1.5A/div.



(a)

$v_s(t)$ 50V/div.
$i_l(t)$ 1.5A/div.
$i_a(t)$ 1.5A/div.
$i_{rh}(t)$ 1.5A/div.



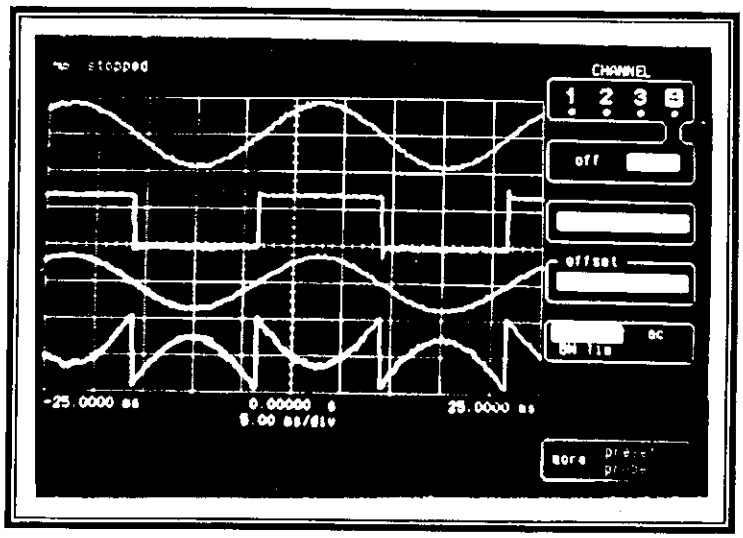
(b)

$v_s(t)$ 50V/div.
$i_l(t)$ 1.5A/div.
$i_a(t)$ 1.5A/div.
$i_{rh}(t)$ 1.5A/div.

(c)

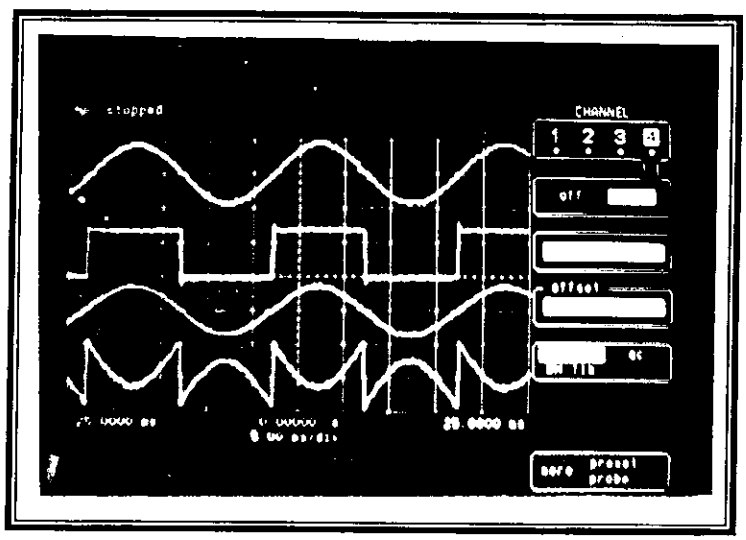
Fig.(4-9): Experimental results of the nonlinear load test. (10 msec./div.) (a) Full wave diodes rectifier with R-L in dc side, (b) Full wave diodes rectifier with R-C in dc side, (c) Half wave rectifier.

$v_s(t)$	3V/div.
$i_l(t)$	1A/div.
$i_a(t)$	1A/div.
$i_{rh}(t)$	1A/div.



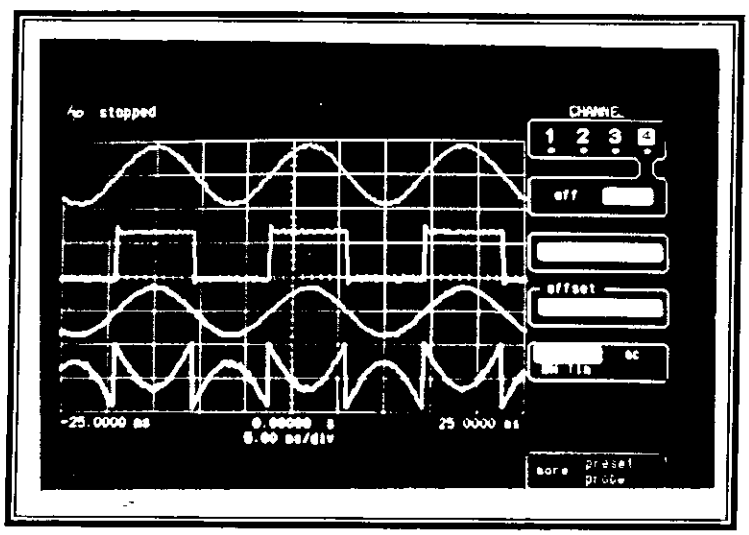
(a)

$v_s(t)$	3V/div.
$i_l(t)$	1A/div.
$i_a(t)$	1A/div.
$i_{rh}(t)$	1A/div.



(b)

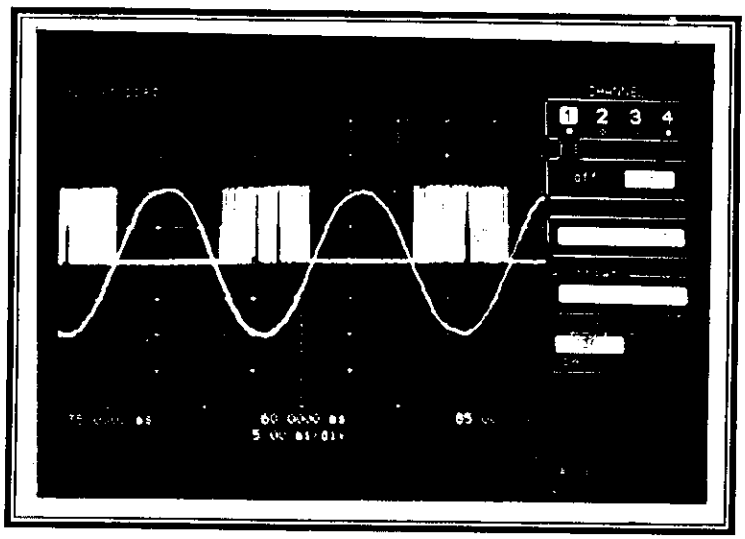
$v_s(t)$	3V/div.
$i_l(t)$	1A/div.
$i_a(t)$	1A/div.
$i_{rh}(t)$	1A/div.



(c)

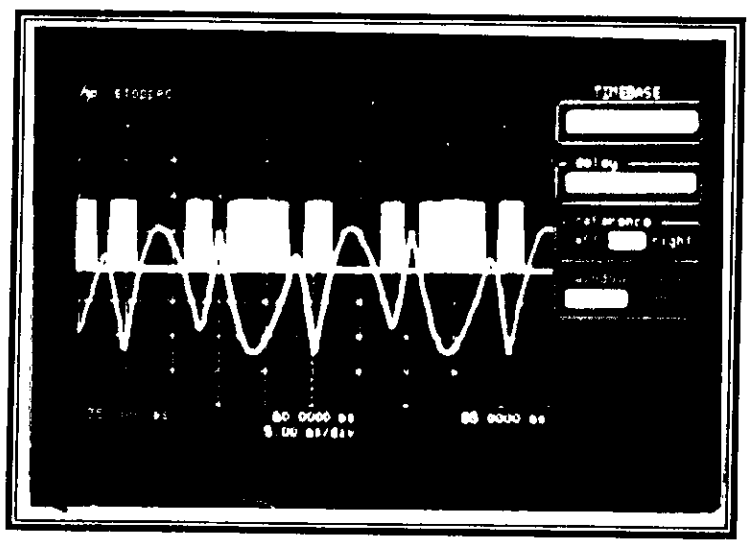
Fig.(4-10): (a), (b) and (c) Experimental results with half wave rectifier load for 40, 50 and 60 Hz respectively. (10 msec./div)

Sine wave
0.5V/div.
Pulses
5V/div.



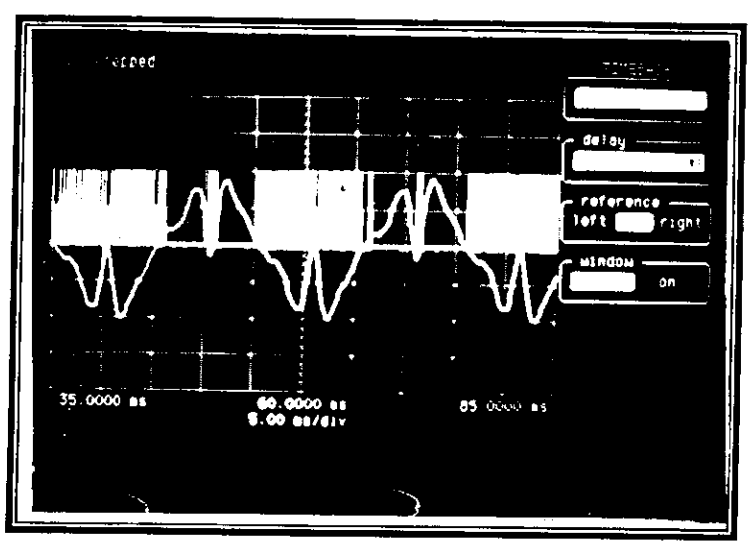
(a)

Non-sinusoidal
wave 0.5V/div.
Pulses
5V/div.



(b)

Non-sinusoidal
wave 0.5V/div.
Pulses
5V/div.



(c)

Fig.(4-11): Experimental results of the drive circuit between reference current and PWM signal with negative part of the reference current only. (a) Linear load, (b) and (c) nonlinear load. (5 msec./div.)

Pulses of T_1

Pulses of T_2

Pulses of T_3

Pulses of T_4

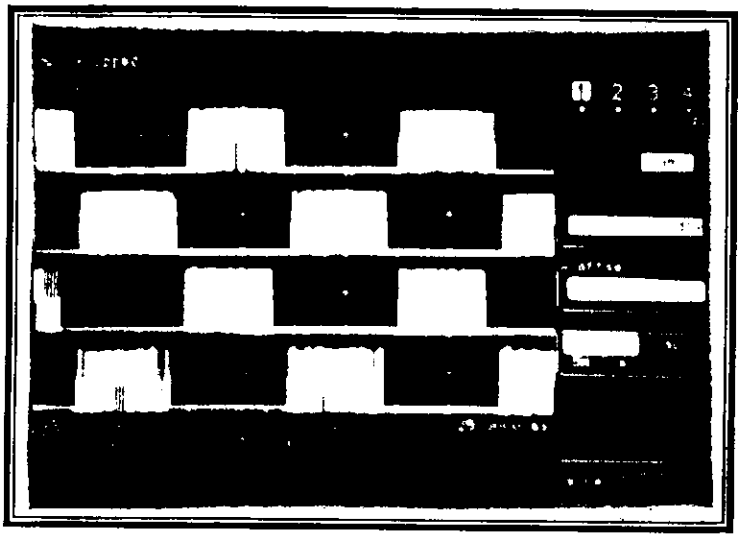
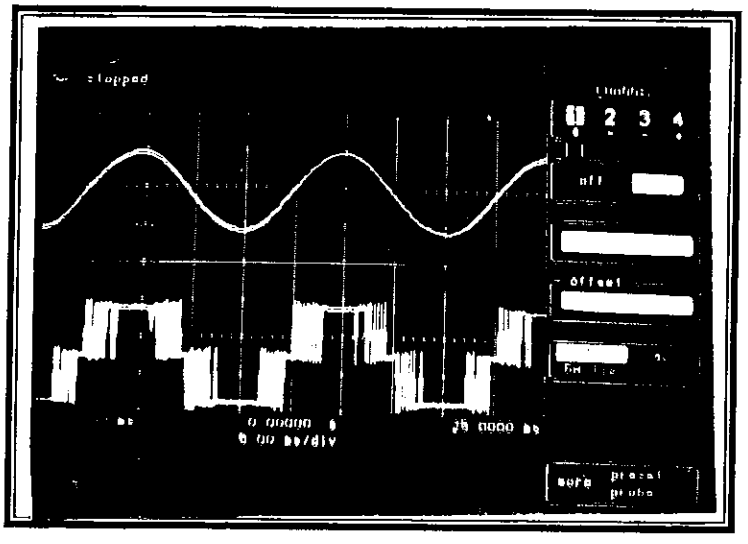


Fig.(4-12): The operating pulses of the signal phase active power filter for linear load (5V/div.). (5 msec./div.)

$i_F(t)$ 1A/div.

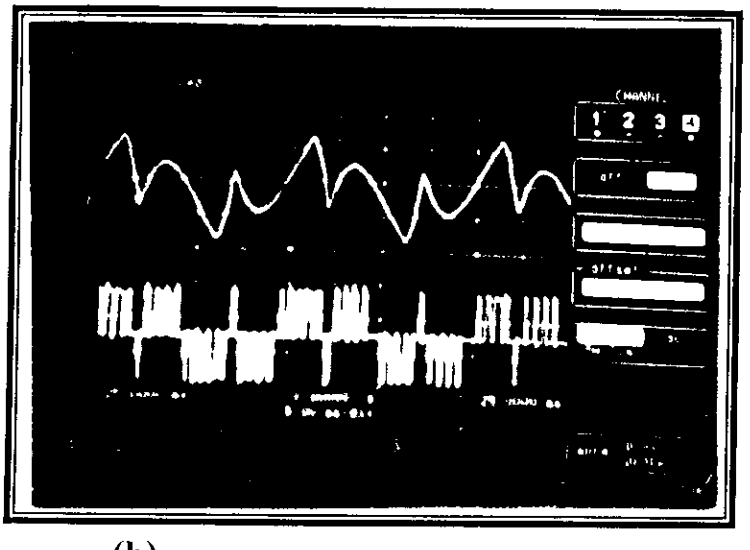
$v_{inv.}(t)$ 50V/div.



(a)

$i_F(t)$ 1A/div.

$v_{inv.}(t)$ 50V/div.



(b)

Fig.(4-13): The compensating current $i_F(t)$ and output voltage $v_{inv.}(t)$ of active power filter (a) Linear load, (b) nonlinear load. (5 msec. / div.)

T_1, T_4

D_1, D_4

D_2, D_3

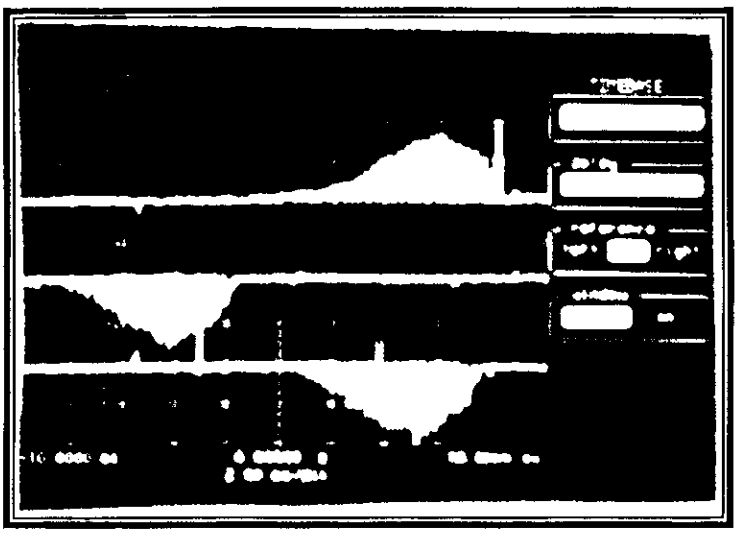


Fig.(4-14): The diodes and transistors current. (5 msec./div.)

phase a

phase b

phase c

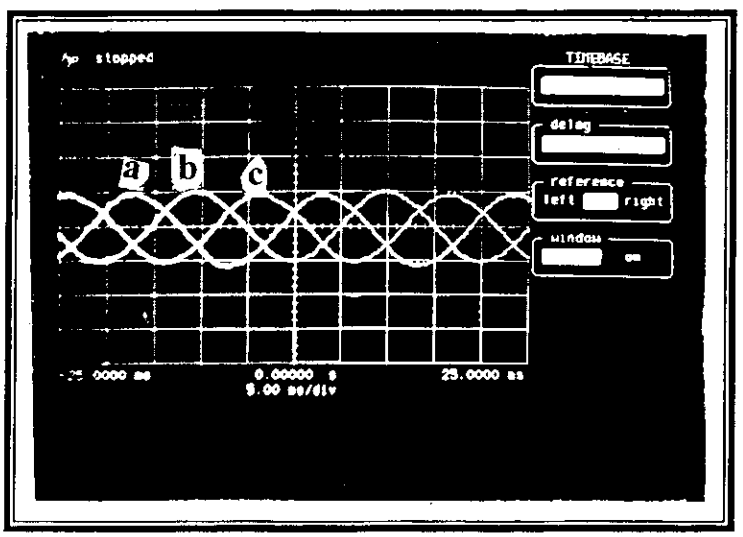


Fig.(4-16): The reference currents of the three-phase system. (5 msec./div.)

Pulses of T_1

Pulses of T_3

Pulses of T_5

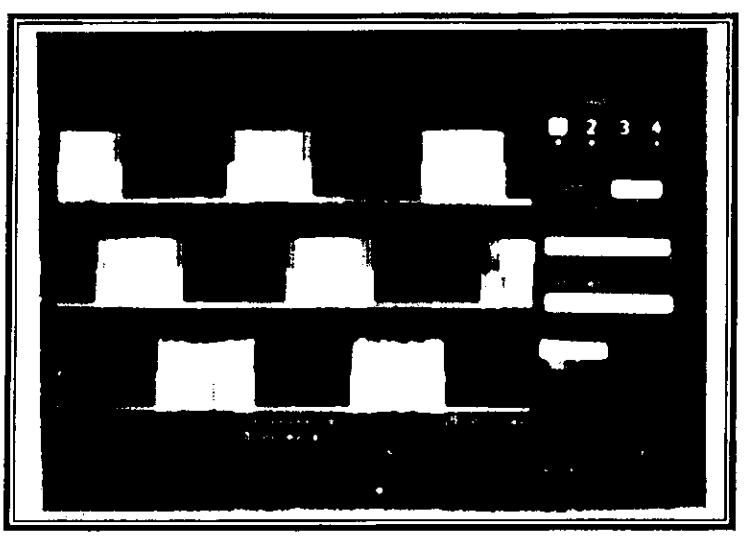
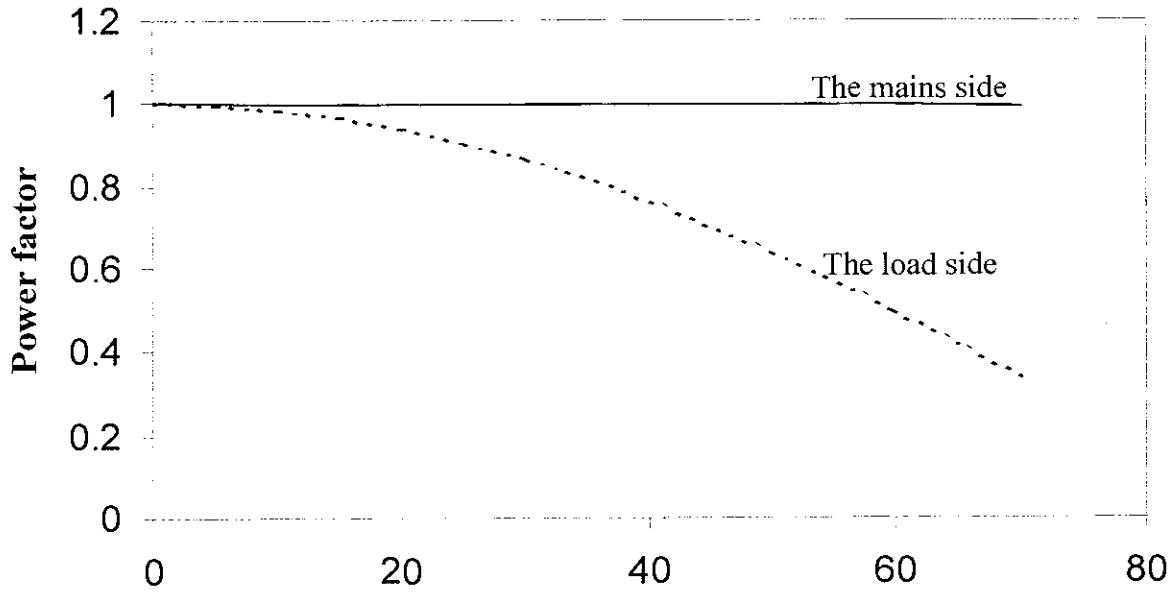
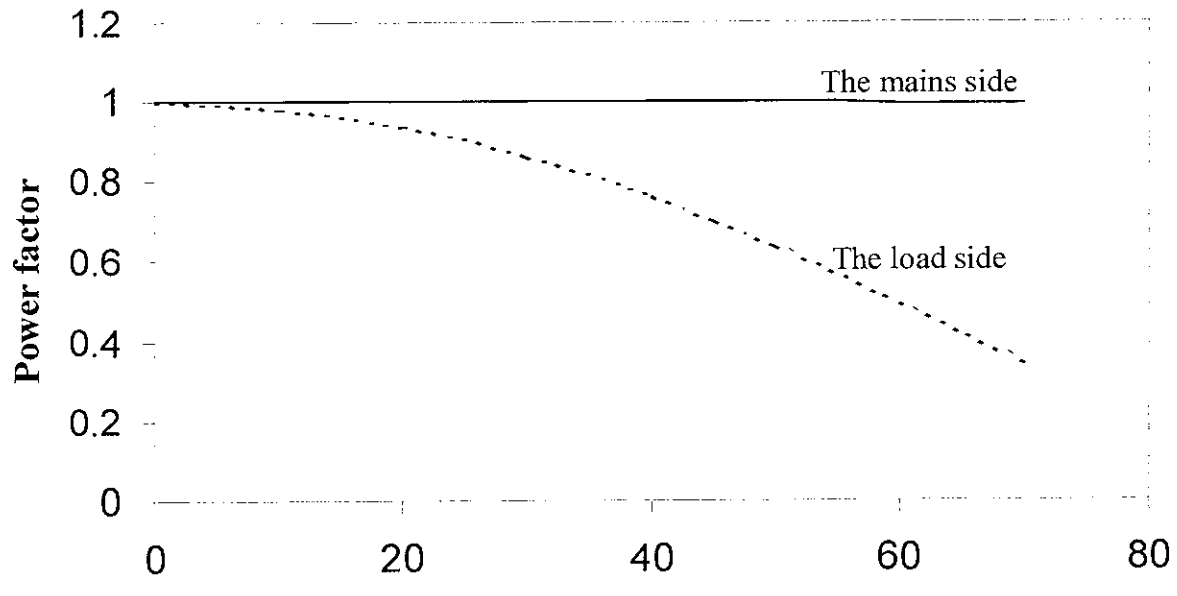


Fig.(4-17): The operating pulses of the three-phase VSI at f=3KHz. (5 msec./div.)

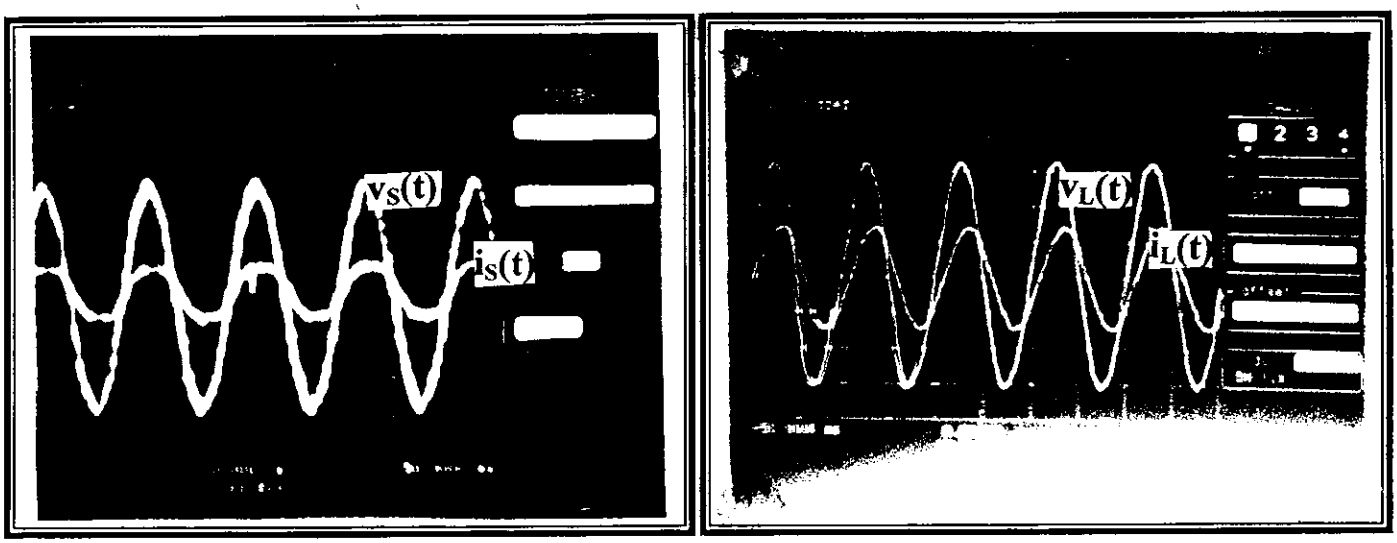


(a)



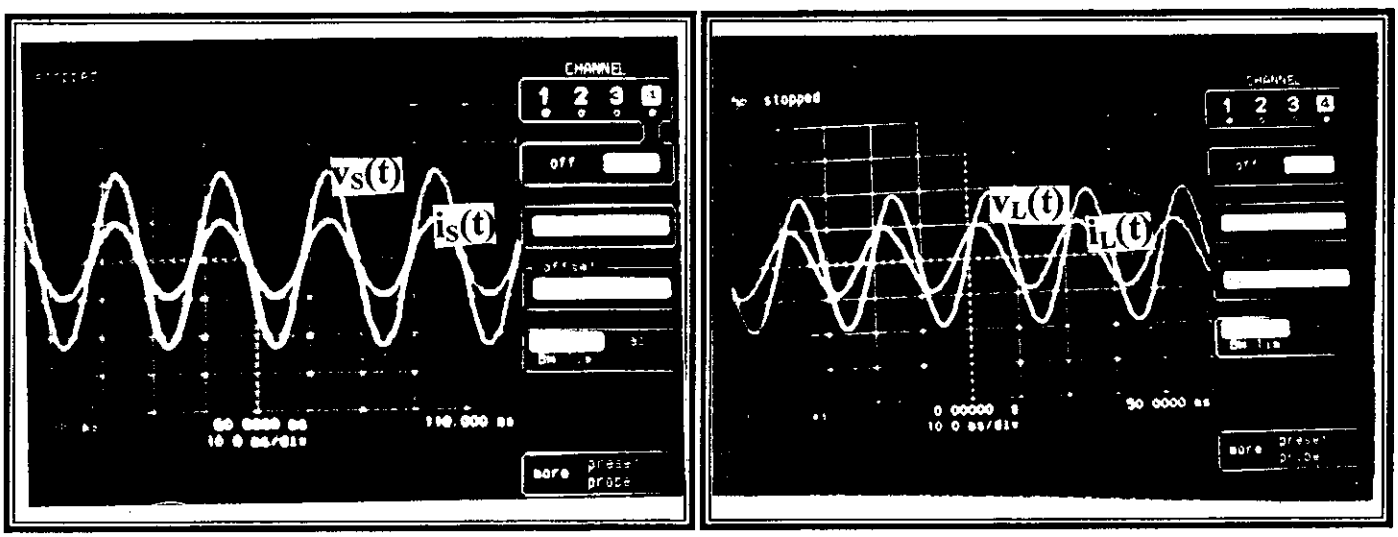
(b)

Fig.(4-18): Change of load power factor and mains power factor for
(a) Inductive load test.
(b) Capacitive load test.



(2) (1)

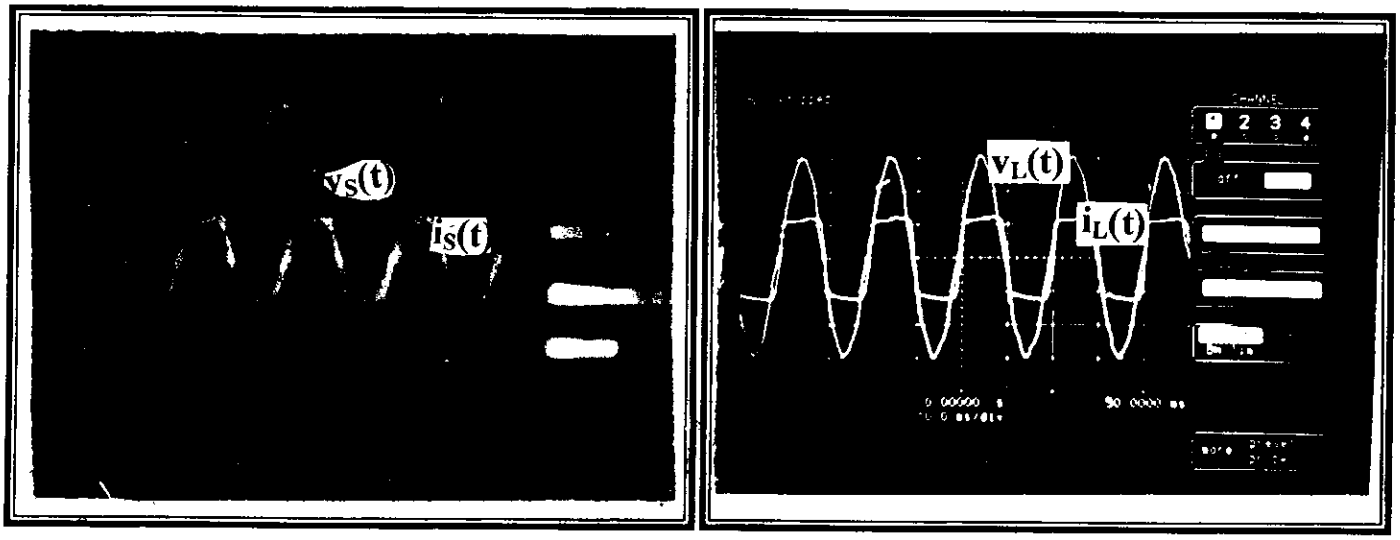
(a)



(2) (1)

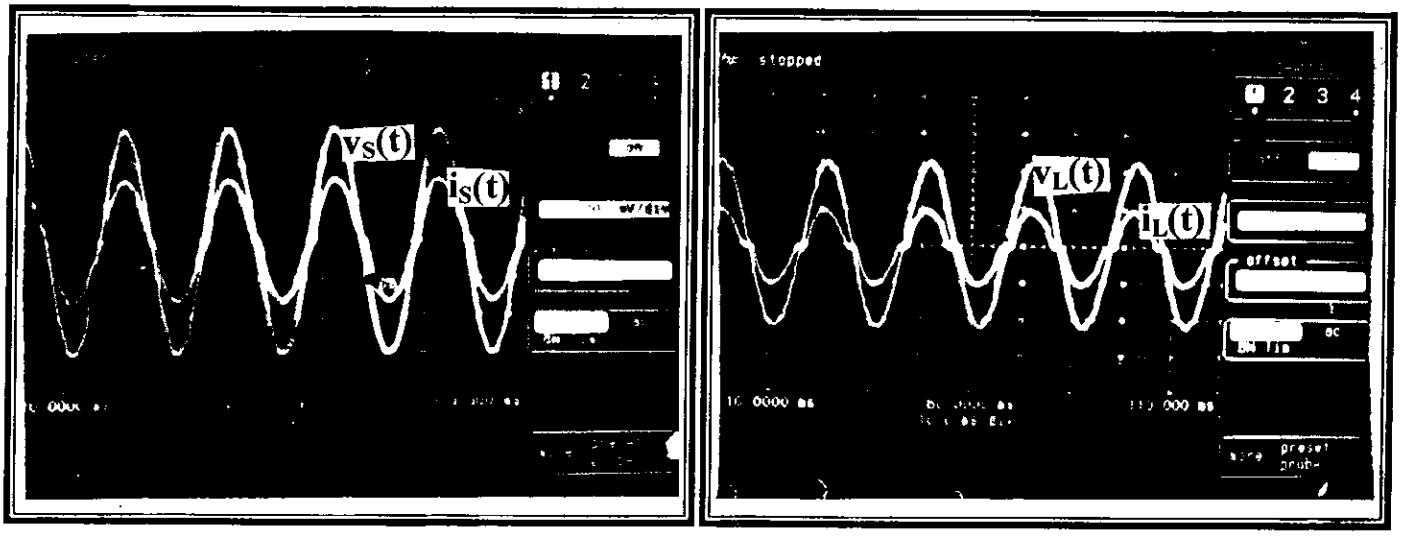
$v_S(t)$, $v_L(t)$ 20V/div. (b) $i_S(t)$, $i_L(t)$ 1A/div.

Fig(4-19): Reactive power compensation performance.(10 msec./div.)
(1) current and voltage of the load.
(2) current and voltage of the mains supply.
(a) Inductive load test, (b) Capacitive load test.



(2) (1)

(a)



(2) (1)

$v_S(t)$, $v_L(t)$ 20V/div. (b) $i_S(t)$, $i_L(t)$ 1A/div.

Fig.(4-20):Harmonics cancellation performance. (10 msec /div.)
(1) current and voltage of the load.
(2) current and voltage of the mains supply.
(a) full wave diode rectifier with R-L load in dc side.
(b) full wave diode rectifier with R-C load in dc side.

CHAPTER FIVE

Conclusions and Future Work

References

The 565 PLL

A-1 The complete configuration of the NE 565 phase locked loop (PLL) is shown in fig. A-1. It is a self contained, adaptable filter and demodulator for the frequency range from 0.001Hz to 500 KHz. This circuit comprises a voltage-controlled oscillator, phase compartor, amplifier and low-pass filter as shown in the block diagram. The center frequency of the PLL is determined by the free ranning frequency of the VCO, this frequency can be adjusted externally with a resistor (R_1) or a capacitor (C_1).

A-2 Absolute maximum ratings

Operating voltage	26v
input voltage	3v p-p
power dissipation	300mw

A-3 Design Formules

Free running frequency of VCO $= \dfrac{1.2}{4R_1C_1}$ in Hz

Lock-range $f_L = \pm \dfrac{8f_o}{V_{cc}}$ in Hz

Capture-range $f_c = \pm \dfrac{1}{2\pi}\sqrt{\dfrac{2\pi f_L}{r}}$

$r = 3.6 * 10^3 * C_2$

A-4 Block Diagram

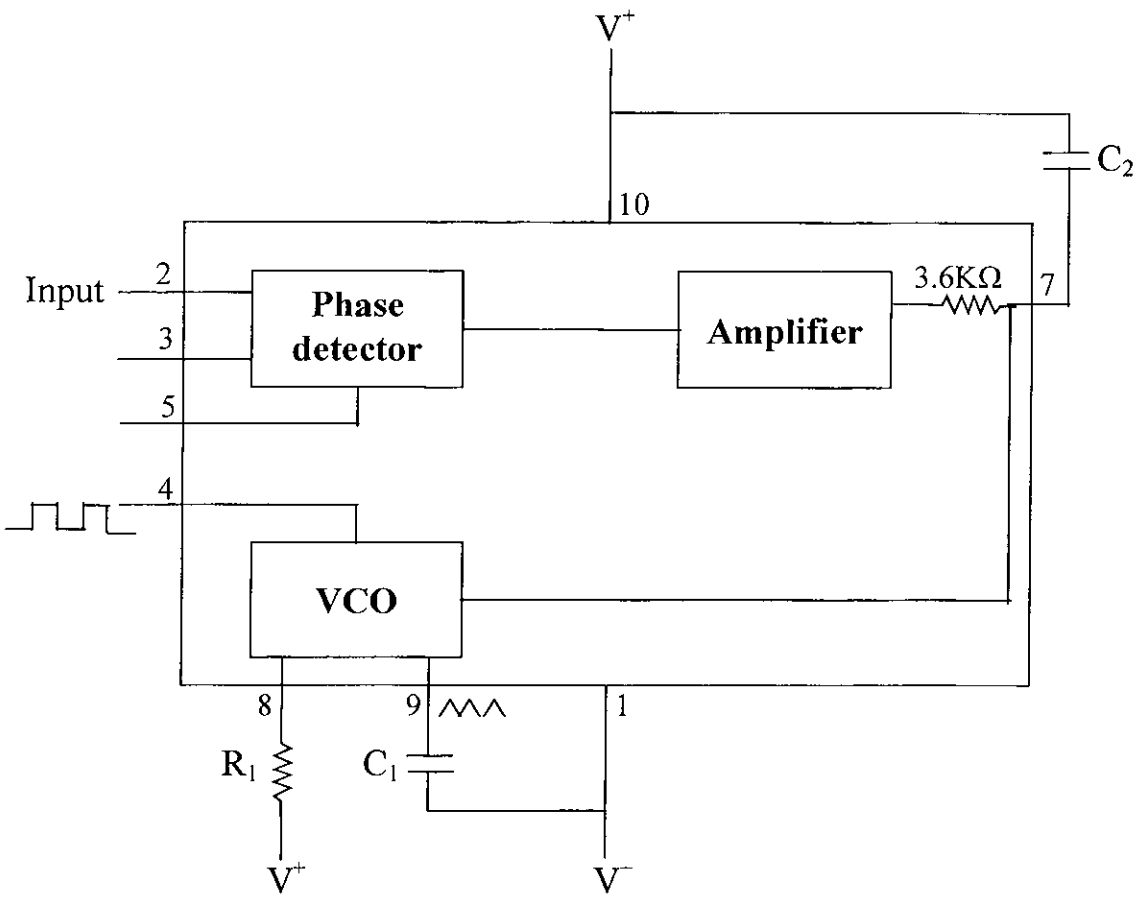


Fig. (A-1): Block diagram of PLL.

Sellection of the P-I controller elements

The transfer function of this controller [40]

$$G(s) = K_P + \frac{K_I}{S}$$

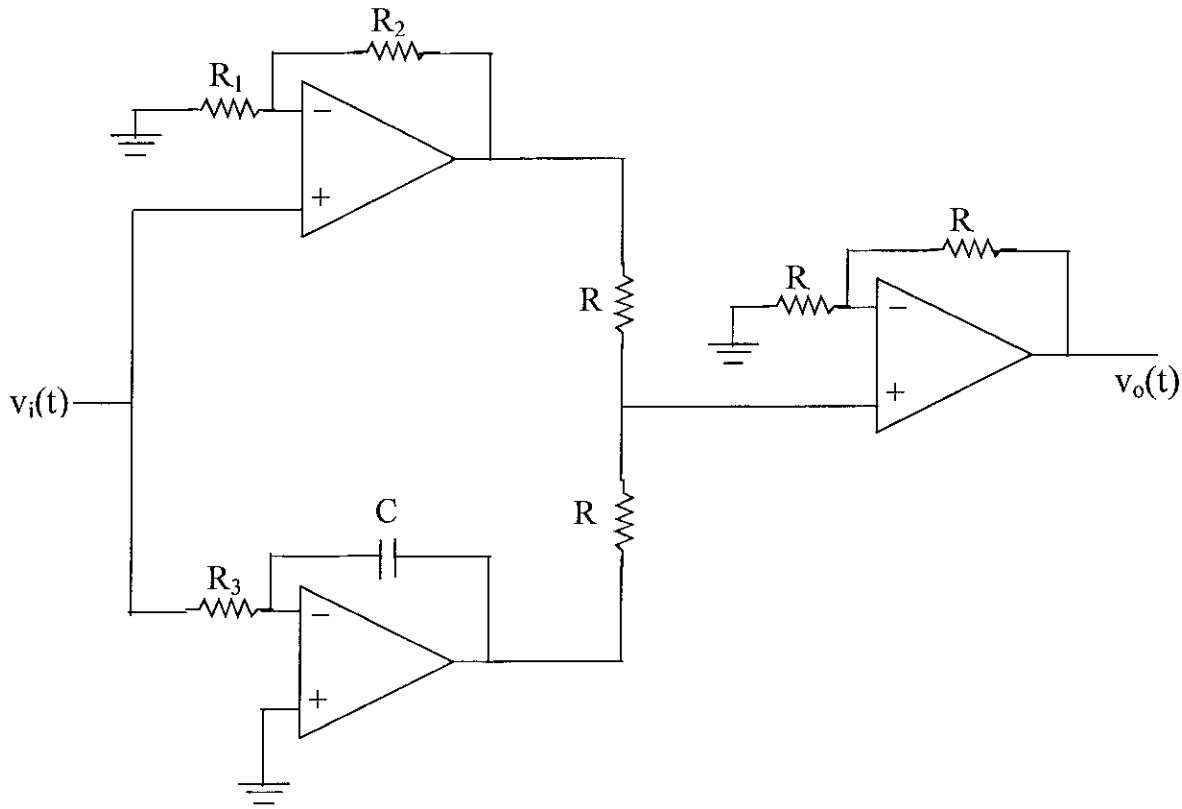


Fig.(C-1): P-I controller.

The parameters of this controller have been elected in section (3.5.1) as (K_P=35 and K_I=400) to obtain optimal response of the system.

From Fig. (C-1).

$$K_P = 1 + \frac{R_1}{R_2}$$

let R_1=34 KΩ then R_2=1 KΩ

Also, $K_1 = \frac{K_P}{R_3 C}$

let R_3=1.5 KΩ then C=10 μF

The optoisalotor device

The optoisalotor (also called an optocoupler) is a device that provides electrical isolation between a two circuit. It is enclosed in a miniature six-pin plastic package as shown in Fig.(D-1). The optocoupler consists of light-emitting diode (LED) on the input and a potosenser at the output. The several optosensor configurations are differ only in type of the photosensor, SCR or traic or transistor of ac power switching applications. In this pototype the 4N36 is used.

The characteristic is following:

The 4N36 consists of emitting diode
coupled with an NPN phototransistor

Input diode	
fourward dc current	90mA
Reverse voltage	3V
Power dissipation 25°C	135mw
Output transistor power dissipation	200mw

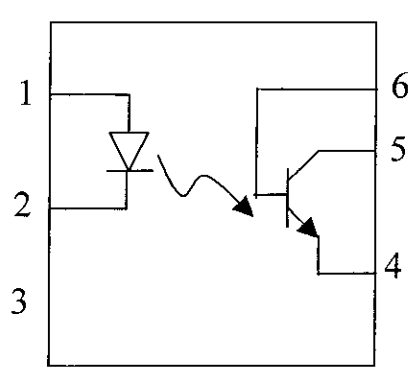


Fig. (D-1): Optoisolator.

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لقد تم بحث و تطوير مرشحات القدرة الفعالة لاستخدامها في تعويض القدرة غير الفعالة (Reactive power compensation) وإزالة التوافقيات (Harmonics elimination) وكذلك للتغلب على مشاكل الطرق التقليدية المستخدمة لإنجاز تلك الأهداف .

في هذا العمل تم تحليل مرشحات القدرة الفعالة أحادية و ثلاثية الطور (Single and three- phase active power filters) من حيث شرح مبدأ العمل و فحص و تطوير معادلات التصميم. هذه المرشحات المُقدمة تستخدم مغير الفولتية (Voltage source inverter) المُسيطر عليه كمصدر للتيار (Current - controlled) باستخدام تقنية تعديل عرض النبضة (Pulse – width modulation).

المرشحات المُنفذة في هذه الدراسة تعمل على توليد القدرة غير الفعالة التي يحتاجها الحمل بالإضافة إلى إزالة التوافقيات وهذه الوظائف أُنجزت بواسطة حقن التيار المناسب بغض النظر عن طبيعة الحمل وتشوهات فولتية المصدر.

دائرة السيطرة (Control circuit) المُستخدمة تمتاز ببساطتها وفعاليتها و قلة كلفتها فهي تحتاج إلى متحسس واحد لتيار الحمل. و كذلك تمتاز بسرعة استجابتها لتغيرات الحمل المفاجئة و وصولها إلى الحالة المستقرة (Steady state) بعد دورتين فقط من زمن موجة تيار المصدر. هذه الدائرة تستطيع العمل بنجاح بمديات من التردد تمتد من 40Hz إلى 60Hz باستخدام دائرة قفل الطور (Phase- (PLL) locked loop) .

في هذا العمل تم أيضاً اشتقاق قوانين السيطرة على المرشحات وأُثبتت النتائج نظرياً بتمثيلها على الحاسبة (Computer simulations) وعمليا بتشغيل النموذج العملي وفحصه مختبرياً (Laboratory tests) .