Multi-Knowledge Electronic Comprehensive Journal For Education And Science Publications (MECSJ)
Issues (55) 2022
ISSN: 2616-9185
www.mecsj.com

Utilizing 45nm, 32nm, and 22nm Technologies in the Evaluation of Gates Simulation by HSPICE

Wael Saad Ahmed

University of Tikrit

E-mail: wael.alrawi@tu.edu.iq

Nabeel Abdulrazaq Yaseen

University of Misan

E-mail: nabil@uomisan.edu.iq

Khaleel Ali Khudhur

University of Northern,Technical College of Kirkuk,

E-mail: Khaleel2012ali@ntu.edu.iq

Multi-Knowledge Electronic Comprehensive Journal For Education And Science Publications (MECSJ)
Issues (55) 2022
ISSN: 2616-9185
www.mecsj.com

Abstract

This article provides a comparison test between various manufacturing technologies for the universal logic circuit used in VLSI. The tool used for this evaluation is the SYNOPSIS tool, an HSPICE used to design fully customized digital circuit simulations. the universal gates are made entirely of CMOS. Various techniques offer different output limits with special information limits. Next, the main logic behind this test is to choose the best strategy for a given number of outcome limits for a given number of information limits for different applications based entirely on gates of rationality. Traditional devices generally consume quite a bit of power and cannot withstand frequency variations. Therefore, a comparative evaluation of using a different technique to design good conventional superior logic is suggested. This comparison is mainly based on the simulation and evaluation method and the power consumption of various logic gates.

Keywords: Circuit Logic, NAND, VLSI, Power, Delay

Multi-Knowledge Electronic Comprehensive Journal For Education And Science Publications (MECSJ)
Issues (55) 2022
ISSN: 2616-9185
www.mecsj.com

1. Introduction

Logic gates are electrical devices that create a logic output from a single input or multiple inputs. Logic gates are used in a variety of applications, from small logic gates to large computers (Chouhan, Chaudhary, Upadhay, Rupani, & Whig, 2017). There are many logic gates that can be used to construct different Boolean logic, but two of them are universal (Mathew, 2004). Charles Sanders Peirce explained in his work that universal logic gates, such as NAND and NOR (Benedetto, 2004), can be used to construct all basic logic gates. However, Henry M. Schaeffer was the first to publish it (Chen & Hsiao, 1984). We have used NAND to investigate how the output changes as a result of different design techniques. hspice was the tool that was used. These can be used for transient circuit analysis as well as AC and DC current analysis. Here are the questions asked:

- ✓ Why is it that NAND is the only option, instead of NOR?
- ✓ What precisely are the diverse design technologies?
- ✓ Why is the Length of Transistors used to categories those technologies?

Multi-Knowledge Electronic Comprehensive Journal For Education And Science Publications (MECSJ)
Issues (55) 2022
ISSN: 2616-9185
www.mecsj.com

2. Only a NAND logical gate is used, not a NOR logical gate.

- ✓ The delay time inside the NAND gate is much shorter than the delay time inside the NOR gate. The delay time is greater than nmos because the pmos chain connection will increase the impedance of the whole circuit.
- ✓ Due to the NAND structure, the specified position is much smaller than the NOR layout. The goal is to achieve a similar channel length for more noticeable current tuning in NOR than in NAND, as the versatility of the apertures is many times not exactly that of electrons.
- ✓ in the NAND structure, the gate leakage current is low.

For NAND gates the scaling of the transistors used for the output is the same for PMOS and NMOS, but for NOR gates the scaling of the transistors used is different.

Multi-Knowledge Electronic Comprehensive Journal For Education And Science Publications (MECSJ)
Issues (55) 2022
ISSN: 2616-9185
www.mecsj.com

3. Different Technologies and The reason for Their expression Along The transistors

Various electronic factor techniques used for simulation or circuit design have predefined manufacturing parameters. For transistors, it depends on the length of the transistor [9-10]. Because current modulation is a characteristic of channel length, the definition technology uses transistor length, not width (Massobrio & Antognetti, 1993).

4. Variety of Logic Gates

4.1 OR Gate

An OR gate is a digital circuit with one high output (1) and one or more high inputs. An OR operation is indicated by a plus symbol (+). (Fig. 1).

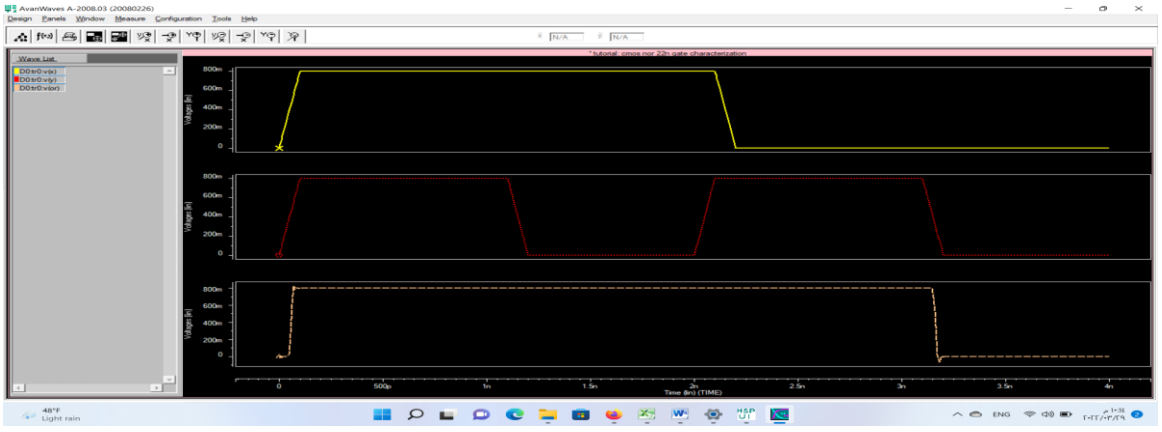

Figure (1). Input / output waveform of the OR gate circuit.

Multi-Knowledge Electronic Comprehensive Journal For Education And Science Publications (MECSJ)
Issues (55) 2022
ISSN: 2616-9185
www.mecsj.com

4.2 NOR Gate

A NOR gate is created when an OR gate and a NOT gate are used together. The output of all NOR gates is low if any of the inputs are high. The code is a small ring at the exit of an OR gate. Reflections are represented as circles (Fig. 2).

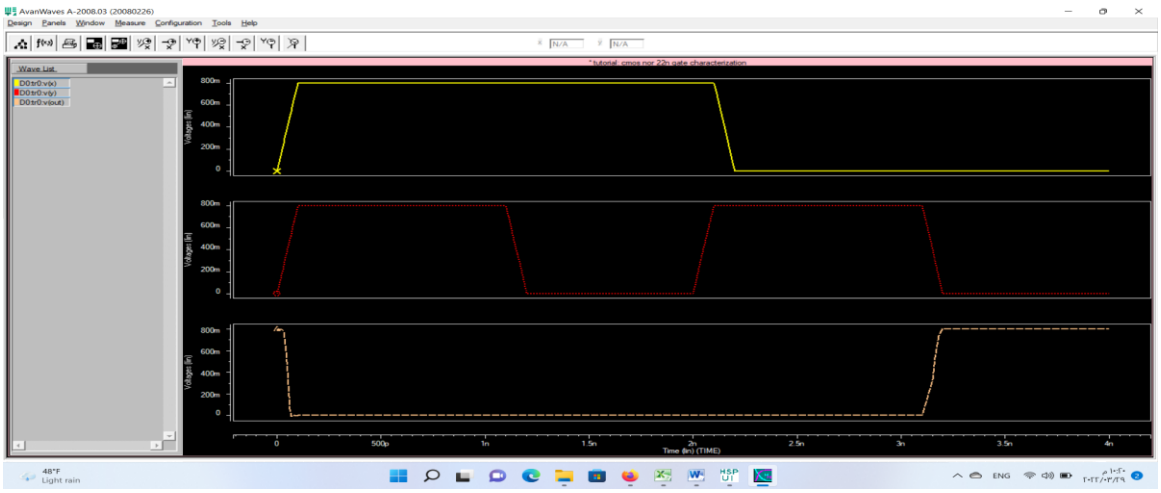

Figure (2). Input / output waveform of the NOR gate circuit.

4.3 AND Gate

Gates are digital circuits that provide high performance (1) specifically if all inputs are high. The period (.) Is used to represent the AND operation, i.e. A.B. Note that this point or AB may be omitted (Fig. 3).

Multi-Knowledge Electronic Comprehensive Journal For Education And Science Publications (MECSJ)
Issues (55) 2022
ISSN: 2616-9185
www.mecsj.com

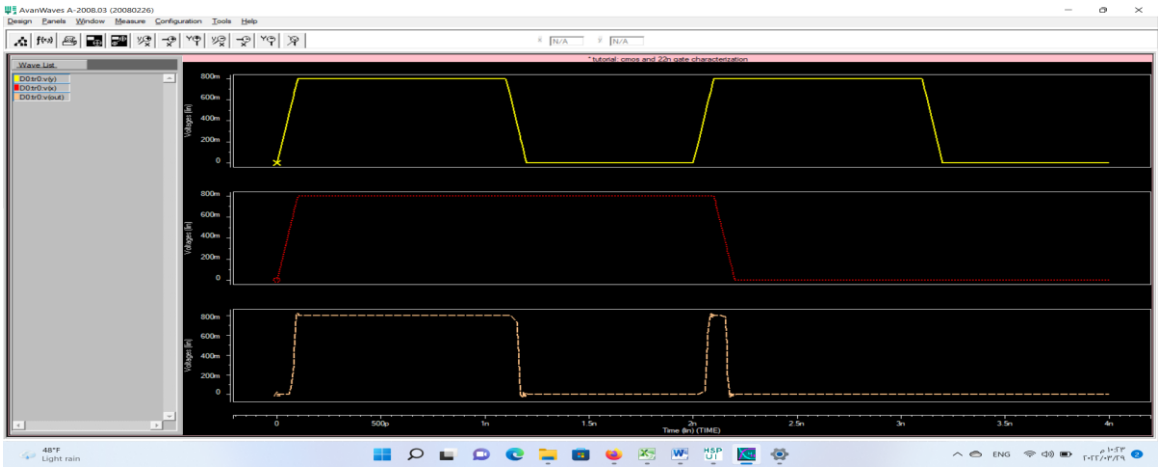

Figure (3). Input / output waveform of the AND gate circuit.

4.4 NAND Gate

This is similar after executing a NAND gate with the help of an AND gate executed with the help of a NOT gate. The output of the full NAND gates is high, while that of the inputs is low. The code is an AND access along with a small outer ring. The association represents the reflex (Fig. 4).

Multi-Knowledge Electronic Comprehensive Journal For Education And Science Publications (MECSJ)
Issues (55) 2022
ISSN: 2616-9185
www.mecsj.com

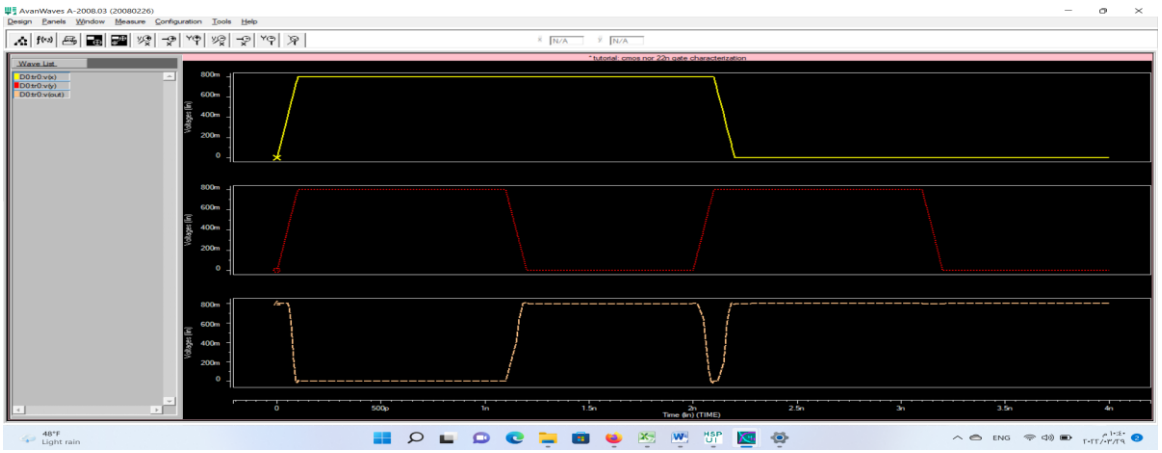

Figure (4) Input / output waveform of the NAND gate circu

4.5. Inverter Gate

The NOT gate is a digital circuit that generates the opposite pattern from input to output. Also known as an investor. The opposite output is called NOT A if the input variable is A. It is also known as A or A with a slash across the top, as shown in the output. The procedures for converting a NAND logic gate to a logic gate are NOT shown in the following diagram. Similarly, NOR logic gates can be used to do this (Fig. 5).

Multi-Knowledge Electronic Comprehensive Journal For Education And Science Publications (MECSJ)
Issues (55) 2022
ISSN: 2616-9185
www.mecsj.com

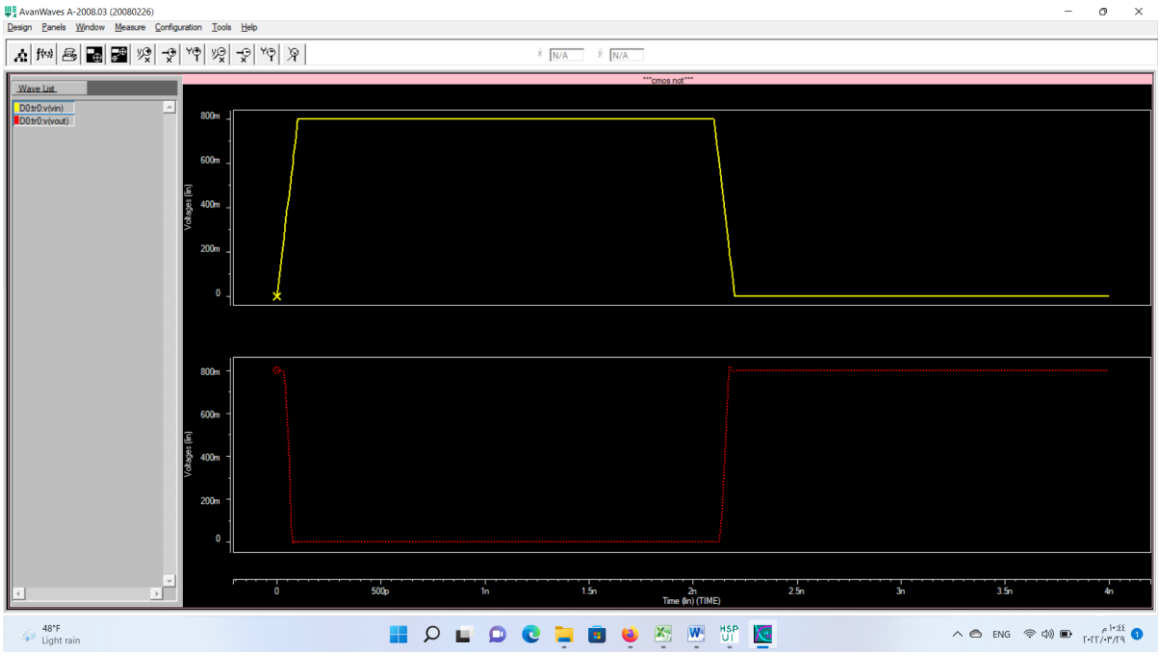

Figure (5). Input / output waveform of the NOT gate circuit

5. Simaltion & Reslut All Circuit

All the aforementioned circuits created with hspice are simulated and some characteristics such as power consumption, delay time, etc. are provided to hspice, which are described in the following tables (1-2).

Multi-Knowledge Electronic Comprehensive Journal For Education And Science Publications (MECSJ)
Issues (55) 2022
ISSN: 2616-9185
www.mecsj.com

Table 1 Energy comparison.

Gate energy comparison with different technologies.				
gate	power	22nm	32nm	45nm
NAND	Maximum power	1.6608E-06	3.9099E-06	9.4358E-06
	Average power	3.8941E-08	7.9154E-08	1.6508E-07
	Minimum power	20.9465E-12	29.9939E-12	270.5150E-12
OR	Maximum power	2.7559E-06	5.9655E-06	1.4364E-05
	Average power	2.8228E-08	5.3004E-08	1.1167E-07
	Minimum power	4.4743E-09	2.3918E-09	1.8481E-09
AND	Maximum power	3.5692E-06	1.0366E-05	2.1462E-05
	Average power	7.7025E-08	1.4894E-07	2.9425E-07
	Minimum power	3.4070E-09	995.9827E-012	688.2490E-12

Multi-Knowledge Electronic Comprehensive Journal For Education And Science Publications (MECSJ)
Issues (55) 2022
ISSN: 2616-9185
www.mecsj.com

NOT	Maximum power	1.5951E-06	3.3392E-06	6.8072E-06
	Average power	1.5568E-08	2.4737E-08	5.1076E-08
	Minimum power	1.4614E-09	995.5609E-12	828.7632E-12
NOR	Maximum power	9.9192E-07	2.8401E-06	5.7799E-06
	Average power	1.8402E-08	3.3169E-08	6.4959E-08
	Minimum power	2.9214E-09	1.9909E-09	1.6575E-09

Multi-Knowledge Electronic Comprehensive Journal For Education And Science Publications (MECSJ)
Issues (55) 2022
ISSN: 2616-9185
www.mecsj.com

Table 2 . time measurement

Time measurement				
gate	measurement	22nm	32nm	45nm
NAND	rise	-1.0001E-09	-1.9950E-09	-9.9372E-10
	fall	2.4413E-11	2.1385E-11	2.2255E-11
	tavg	-4.8783E-10	-9.8681E-10	-4.8573E-10
OR	rise	1.0104E-09	1.0132E-09	1.0142E-09
	fall	2.7243E-12	2.8081E-12	1.1968E-12
	tavg	5.0657E-10	5.0801E-10	5.0772E-10

Multi-Knowledge Electronic Comprehensive Journal For Education And Science Publications (MECSJ)
Issues (55) 2022
ISSN: 2616-9185
www.mecsj.com

AND	rise	-3.0678E-09	-3.0677E-09	-3.0696E-09
	fall	1.1114E-09	1.1137E-09	1.1102E-09
	tavg	-9.7821E-10	-9.7700E-10	-9.7968E-10
NOT	rise	2.1023E-12	4.5081E-12	3.7517E-13
	fall	6.0333E-12	5.5332E-12	4.7652E-12
	tavg	4.0678E-12	5.0206E-12	2.5702E-12
NOR	rise	4.0001E-09	4.0036E-09	4.0020E-09
	fall	-4.5890E-12	-5.9778E-13	-1.5436E-12
	tavg	1.9978E-09	2.0015E-09	2.0002E-09

Multi-Knowledge Electronic Comprehensive Journal For Education And Science Publications (MECSJ)
Issues (55) 2022
ISSN: 2616-9185
www.mecsj.com

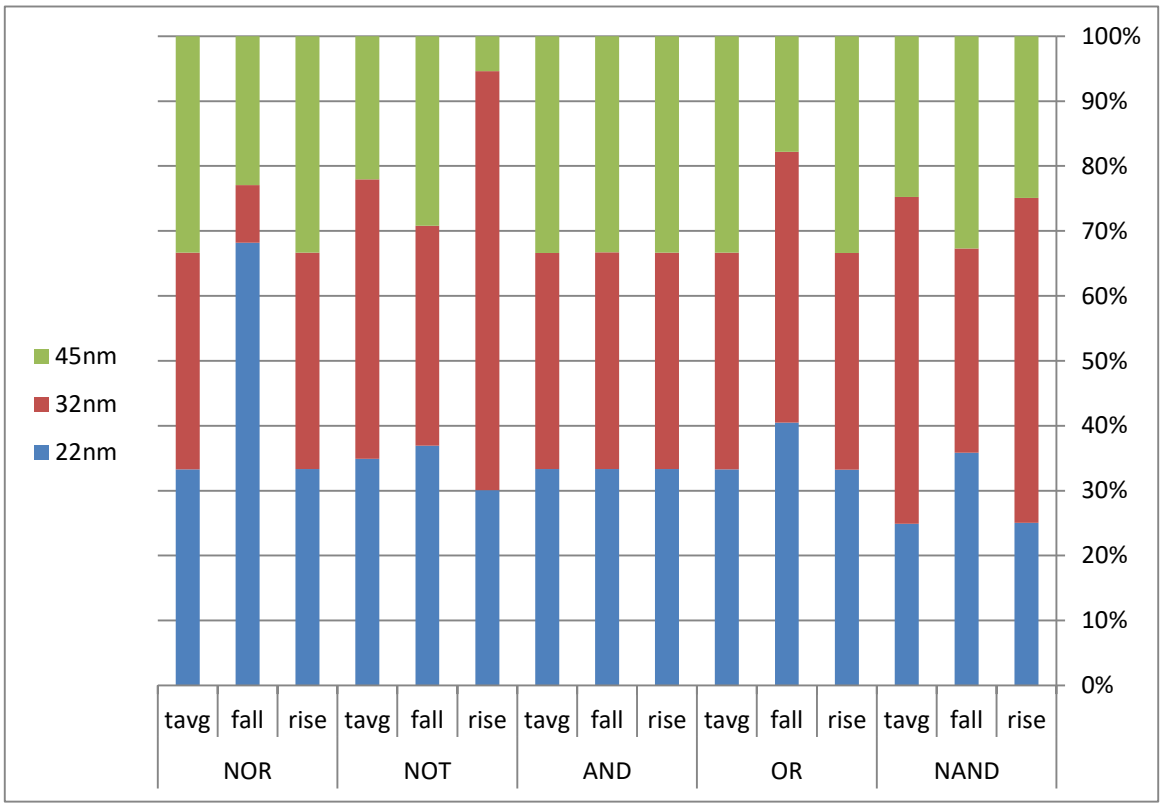

Figure (6). time measurement of all gates with rise. Fall and average.

Multi-Knowledge Electronic Comprehensive Journal For Education And Science Publications (MECSJ)
Issues (55) 2022
ISSN: 2616-9185
www.mecsj.com

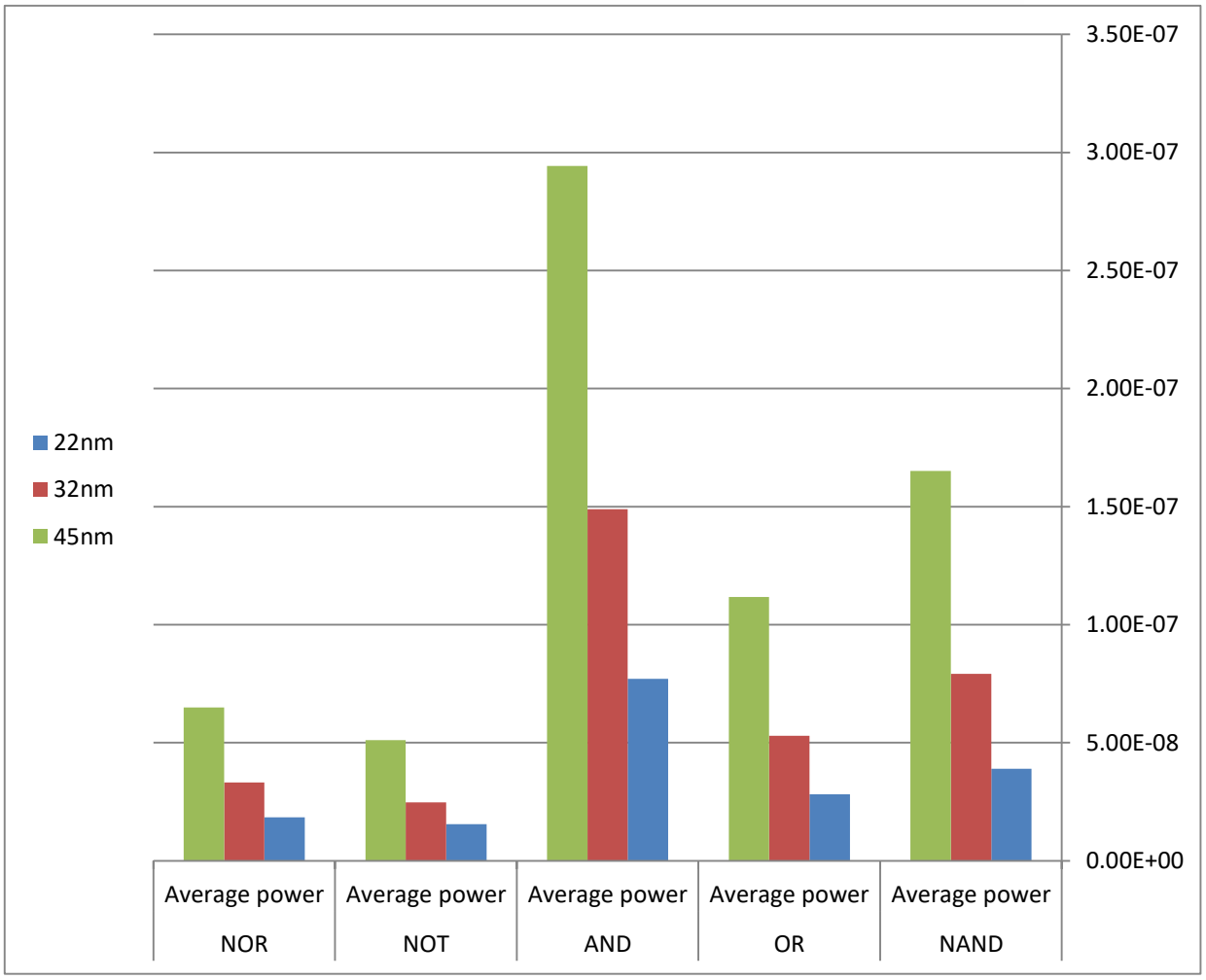

Figure (7). Average performance of all Gates using 22nm, 32nm and 45nm technologies.

Multi-Knowledge Electronic Comprehensive Journal For Education And Science Publications (MECSJ)
Issues (55) 2022
ISSN: 2616-9185
www.mecsj.com

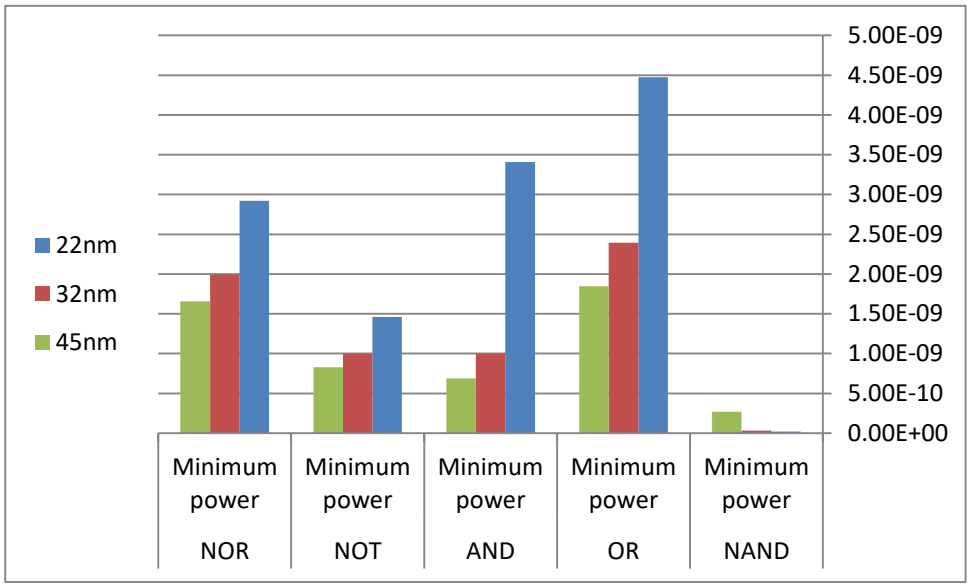

Figure (8). The maximum power of all gates with 22 nm, 32 nm, 45 nm techniques.

Multi-Knowledge Electronic Comprehensive Journal For Education And Science Publications (MECSJ)
Issues (55) 2022
ISSN: 2616-9185
www.mecsj.com

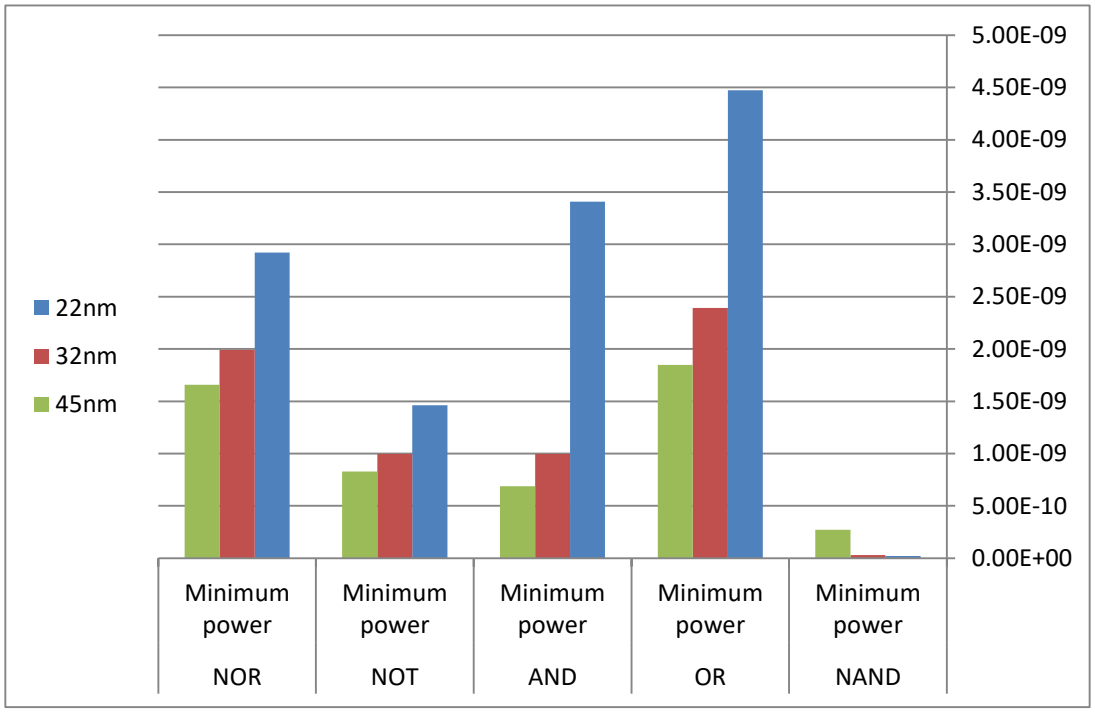

Figure (9). The minimum power of all gates with 22 nm, 32 nm, 45 nm techniques

6. THE RESULTS ARE GRAPHICALLY REPRESENTED.

For better representation, the effects are presented in the form of a line graph (Figure 6-9).

Multi-Knowledge Electronic Comprehensive Journal For Education And Science Publications (MECSJ)
Issues (55) 2022
ISSN: 2616-9185
www.mecsj.com

7. conclusion

The study's findings may be summarized as follows

- ✓ It is imagined that when the size of a semiconductor is reduced, the normal energy usage will increase as the base power consumed increases while most of the power consumed will decrease. The most extreme power is greater and the base power is lowest at 22nm.
- ✓ Technology Compared to various gates and technologies, the NAND gate has the lowest peak power ratio at 45nm.
- ✓ As the volume is reduced as little as possible, the decay time decreases. Since the rise time of the NAND gate is affected by technology, the total transit time of the NAND gate is less than that of other gates.
- ✓ 45nm technology has the shortest rise time and the smaller the size, the shorter the fall time, resulting in a minimum total transit time at 45nm compared to alternative technologies.

Multi-Knowledge Electronic Comprehensive Journal For Education And Science Publications (MECSJ)
Issues (55) 2022
ISSN: 2616-9185
www.mecsj.com

References

- Chouhan S, Chaudhary S, Upadhay T, et al. Comparative study of various gates based in different technologies. Int Rob Auto J. 2017;3(1):262-269. DOI: 10.15406/iratj.2017.03.00046
- L. Mathew et al., "CMOS Vertical Multiple Independent Gate Field Effect Transistor (MIGFET)," 2004 IEEE International SOI Conference (IEEE Cat. No.04CH37573), 2004, pp. 187-189, doi: 10.1109/SOI.2004.1391610.
- J. Benedetto et al., "Heavy ion-induced digital single-event transients in deep submicron Processes," in IEEE Transactions on Nuclear Science, vol. 51, no. 6, pp. 3480-3485, Dec. 2004, doi: 10.1109/TNS.2004.839173.
- C. L. Chen and M. Y. Hsiao, "Error-Correcting Codes for Semiconductor Memory Applications: A State-of-the-Art Review," in IBM Journal of Research and Development, vol. 28, no. 2, pp. 124-134, March 1984, doi: 10.1147/rd.282.0124.
- Massobrio G, Antognetti P. Semiconductor Device Modeling with SPICE. 1993.