DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

FPGA Implantation of Matrix Processing Cores

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Abstract

Currently, to achieve real time performance, a Floating point representation has been important in many fields, especially, in digital signal processing, image processing as well as satellite navigation systems, complex control systems, etc. the real conditions of matrix Multiplication and the Addition of Floating point numbers are considered a big challenge to satisfy, as the process of Multiplication and Addition Floating point numbers are distinguished by high complexity, large chip area density and the extra time needed to the handle data. Therefore, it is recommended that the time might be reduce to gain better performance.

This project analyse and tests four different designs for matrix multiplication and Addition with different representation by using VHDL language to program FPGAs in a virtual environment provided by Xilinx because FPGAs offer decreased costs and a shorter development time. Additionally, their flexibility enables field upgrade and the adaptation of hardware to run-time conditions [3]. This project aimed to implement integer and double precision floating point 64 bits with IEEE 754 Standard in VHDL and simulat the result using the Modelsim program.