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FPGA BASED FUZZY LOGIC CONTROLLER FOR MULTICONVERTER IN DC DISTRIBUTED POWER SYSTEMS

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ETHICAL STATEMENT

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(Ph.D. Thesis)

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ABSTRACT

DC distributed power system is a perfect solution for integrating renewable energy sources because many of these sources usually are DC sources. They are also provided fewer transformation levels of voltage, higher current capacity, and more protection from a short circuit. The voltage level is changed by connecting the converters in series or parallel connections and known as the multiconverter system. A multiconverter system has a large variety of operation instructions because of the interconnection of a large number of power electronic devices in parallel, cascade, and isolating configurations for loads and sources to achieve the required operation. Hence, some converter behaves as a constant power load (CPL). The CPL has a high degree of nonlinearity and exhibits incremental negative resistance (INR) properties. Thus, the INR makes the system low damping and instability and may be led the system to go to failure. This thesis introduces the fuzzy logic controller (FLC) as a new solution to cancel or mitigate the instability effects of CPL. An essential property of FLC is to deal with the nonlinearity of the CPL. the FLC is applied to the buck converters with CPL, and the results are obtained by using FPGA in the loop in the Matlab/Simulink. Additionally, experimental results are obtained by using the buck converter and FPGA based fuzzy logic controller. Results show that FLC has the ability to cancel the instability effects of CPL and keep the output voltage of the source converter to match its reference value. Also, the FLC has a good response against voltage transient and load variations.

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DA DAĞITIK GÜÇ SİSTEMLERİNDE ÇOKLU DÖNÜŞTÜRÜCÜ İÇİN FPGA TABANLI BULANIK MANTIK DENETLEYİCİ

(Doktora Tezi)

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ÖZET

Yenilenebilir enerji kaynaklarının çoğu DA (Doğru Akım) kaynağı olduğu için DA dağıtık güç sistemine bu kaynakları entegre etmek mükemmel bir çözümdür. Ayrıca daha az gerilim dönüşümü, daha yüksek akım kapasitesi ve kısa devre durumunda yüksek koruma sağlarlar. Gerilim seviyesi, dönüştürücülerin seri veya paralel bağlanmasıyla değiştirilir. Bu sistemler kademeli dönüştürücü sistemi olarak bilinir. Kaskad dönüştürücü sistemi, yük ve kaynakların gerekli olduğu şekilde çalışmasını sağlamak için çok sayıda güç elektroniği cihazının birbirine paralel, kaskad ve yalıtılmış şekilde bağlanması nedeniyle çok çeşitli çalışma özelliğine sahiptir. Bu nedenle, bazı dönüştürücüler sabit güçlü bir yük gibi davranır. Sabit güçlü yük, yüksek derecede doğrusal olmayan bir yapıya sahiptir ve artımlı negatif direnç özellikleri gösterir. Böylece, artı negatif direnç sistemi düşük sönümlemeli ve kararsız yapar ve sistemde arızaya neden olmaktadır. Bu tezde, bulanık mantık denetleyicisini sabit güç yükünün kararsızlık etkilerini yok etmek veya azaltmak için yeni bir çözüm yöntemi olarak tanıtılmaktadır. Bulanık Mantık Denetleyicisinin(BMD) önemli bir özelliği, sabit güç yükünün doğrusal olmama durumuyla ilgilenmesidir. BMD, ilk olarak, sabit güç yükü ile çalışan DA-DA alçaltan ve yükselten dönüştürücülere uygulanmış ve Matlab/Simulink'teki FPGA döngüsü kullanılarak sonuçlar elde edilmiştir. Bunlara ek olarak, alçaltan dönüştürücü ve FPGA tabanlı bulanık mantık denetleyicisi kullanılarak deneysel sonuçlar elde edilmiştir. Sonuçlar, bulanık mantık denetleyicinin sabit güçlü yükün kararsızlık etkilerini önleme ve kaynak dönüştürücünün çıkış gerilimini referans değerine yakın tutma yeteneğine sahip olduğunu göstermektedir. Ayrıca, BMD gerilimin geçici etkilerine ve yük değişimlerine karşı iyi bir tepkiye sahiptir.

Bilim Kodu	:	90513
Anahtar Kelimeler	:	Çoklu Dönüştürücü, Bulanık Mantık, Sabit Güçlü Yük, Verilog
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LIST OF ABBREVIATIONS

Abbreviations and symbols which are used in this thesis are elaborated down-below

Symbols	Meanings
C	Capacitor
C_d	Damping capacitor
d	Duty cycle
D	State of duty cycle
$\tilde{d}$	Variable state of duty cycle
dt	Time variation
e	Error
e'	Variation of error
I	Current
i_C	Capacitor current
I_{CPL}	Constant power load current in the experimental results
i_{CPL}	Constant power load current
I_L	Load converter current in the experimental results
i_L	Inductor current
i_o	Output current
I_R	Resistive load current in the experimental results
I_{ref}	Reference current
I_{Ref}	Reference current
K_d	Derivative gain
K_i	Integral gain
K_p	Proportional gain
K_u	Critical gain
L	Inductance

Symbols	Meanings
L_d	Damping inductance
P	Power
P_{CPL}	Power of constant power load
P_{in}	Input power
P_{out}	Output power
R	Resistance
R_{CPL}	The resistance of constant power load
R_d	Damping resistance
R_{equ}	Equivalent resistance
R_f	Filter resistance
r_{in}	Variable state of input resistance
R_L	Load resistance
S_1, S_2	Power electronic switches
T	Cycle period
t	Time
t_{off}	Off-switching time
t_{on}	On-switching time
T_u	Oscillation period
u	Control function
V	Voltage
V_C	Capacitor voltage
v_C	Variable state of capacitor voltage
V_L	Load converter voltage in the experimental results
$V_{meas.}$	Measurement voltage
v_o	Variable state of output voltage
V_o	Output voltage

Symbols	Meanings
$V_{ref.}$	Reference voltage
V_S	Load converter voltage in the experimental results
x_{rang}	The universe of discourse range
Z	Impedance
β	The gain factor of fuzzy logic control
Δi_o	The difference in output current
Δv_o	The difference in output voltage
μ	Membership-value

Abbreviations	Meanings
AC	Alternative current
ADC	Analogue to digital converter
ALU	Adaptive logic module
ASIC	Application specific integrated circuit
CCM	Continuous conduction mode
CLB	Configurable logic blocks
CPL	Constant power load
CVL	Constant voltage load
DC	Direct current
DCM	Discontinuous conduction mode
DSP	Digital signal processing
DTC	Direct torque control
EDA	Electronic design automation
HDL	Hardware description language
HEV	Hybrid electric vehicle
FLC	Fuzzy logic control
FIL	Field programmable gates array in the loop
FPGA	Field programmable gates array

Abbreviations	Meanings
IGBT	Insulated gate bipolar transistor
INR	Incremental negative resistance
IRC	Input-resistance compensator
JTAG	Joint test action group
LPF	Low pass filter
LUT	Look-up table
M	Motor
MES	More electric ship
mf	Membership function
MOSFET	Metal oxide semiconductor field-effect transistor
NB	Negative big membership function
NS	Negative small membership function
PB	Positive big membership function
PI	Proportional integral
PLD	Programmable logic devices
PMSM	Permanent magnet synchronous motor
PS	Positive small membership function
PWM	Pulse width modulation
SSD	Solid-state defender
VHDL	The very high-speed integrated-circuit hardware description language
Z	Zero membership function

1. INTRODUCTION

Distributed generations cover renewable energy sources like a PV system, a wind power system or micro-turbine systems, and storage systems like a fuel cell system [1-5]. The output energy (magnitude and form of current and voltage) from distribution generating is not suitable for use by consumers because it is affected by environmental conditions, and the DGs cannot connect directly to buses of the distribution grid [6-8] Therefore, DGs connect to the main bus by the interfacing converters to convert the output power (voltage and current) utility-grade for an AC or DC system with the desired magnitude voltage and current, and frequency for an AC system [8, 9]. The concept of the DC distributed power system becomes suitable and attractive due to power electronic converter facilities, in which it overcomes some difficulties found in the traditional AC network like power loss in transformers and long transmission lines, and high voltage transformation [7].

Distributed multiconverter power systems have an important role, which allows providing a multi-level voltage for different types of dc or ac loads. At present, there are many examples of these systems spacecraft, modem aircraft, microgrids, More Electric Ship (MES) power, International Space Station, submarine, etc. have many converters in their structures, and the number of converters varies from a few to hundreds in parallel, cascade, stacking, and splitting configurations for loads and source to achieve proper required operation [10, 11]. The converter's connections in distributed multiconverter power systems are cascade, which is a basic configuration of multiconverter. It consists of two or more converters in series connection, the first and the second converter are the source and load stages, respectively [12, 13]. One multiconverter power electronic type is the cascade system of a converter, which consists of a source converter that provides the regulated voltage to the system (others are called upstream converters or voltage regulators) and a second converter that converts the line voltage to proper value and frequency for each load [14, 15]. A multi converter has a large variety of operation instructions because of the interconnection of components of the cascade converter [16-18].

The load converters (second stage of multi converter) tend to display the properties of a constant power load when control is applied tightly[15, 18], which means a converter has a

fast response and low output ripple [16]; therefore, the converter behaves as the CPL with their control bandwidth [19].

CPL means: the load converter takes its power from the main bus, which is constant with any value of current and voltage [18, 20]. CPL has a negative incremental impedance effect, which impacts the power quality of the system and brings instability, which eventually may lead the system into oscillation or failure and stress or damage the system equipment [21]. This issue attracted the attention of researchers and introduced many solutions to cancel or compensate for the instabilities caused by CPL.

Because of the non-linearity and time dependency of converters' operation and the incremental negative impedance effects of constant power loads, classical linear control methods (like a conventional proportional-integral PI controller) have stability limitations around the operating points and do not apply to these systems. Therefore, digital and nonlinear stabilizing control methods must be used to ensure large-signal stability [14, 17, 18, 22-25]. Compensation Techniques of the instability of CPL can be achieved by adding an extra element like passive elements or devices to the power system or redesigned the control loop of a source or load converter [26, 27] such as active damping [20, 28, 29], feedback linearization [30], sliding mode control [31-33], and Lyapunov redesign control [13] have been aimed to remodel the feedback controller of source converter to face instability effects of CPL.

Most of the methods mentioned previously need to obtain exact mathematical parameters of the system. Sometimes this is difficult for calculations because of the nature of a system that is characterized by the nonlinearity and variation of elements of the system [22].

In this thesis, the fuzzy logic control (FLC) is used to compensate for the destabilizing effect of the constant power load under the load variations. The Fuzzy logic controller, whose concept was introduced by Lotfi Zadeh in 1965, has many applications in the power system. For example, the power system stability control, the power system stability assessment, and the process optimization for generation, transmission, and distribution. Fuzzy logic is also used in motion control, motor efficiency optimization, and waveform estimation [23]. The reason for the use of FLC in power systems is that it has the following advantages: FLC does not need accurate mathematical models when managing the system. Therefore, fuzzy logic

control is useful for an extensive system that has a problematic mathematical model. FLC is dependent on deduction so that it can incorporate human intuition and experience [23-25]. Because of the nonlinearity of the power electronics converter and where the sensor signals are not accurate, the FLC is a well-controlled approach to overcome these issues. FLC has a robust performance under parameter variation and loads disturbance effect due to the natural properties of FLC, nonlinear, and adaptive [24, 25].

The motivation of this work is to design the fuzzy logic control as a new solution for a multi converter system with different types of load in the DC distributed power system on the FPGA board. It is introduced the design, simulate and implement the fuzzy logic controller for a cascade system that has a multiconverter with a constant power load. A five memberships functions map the error and variation of the error to regulate and stabilize the output voltage of the source converter, which is feeding different types of load, constant voltage load, load converter, and CPL through primary DC voltage.

Also, it is introduced the implementation of the fuzzy logic and the intelligent PWM chip by using the FPGA board. The input data of FPGA are 12-bit A/D for output, and reference voltages and output is required duty cycle, as shown in Figure 1.12. The simulation results obtained by using FPGA in the loop on Matlab/Simulink Environment. Also, the FLC used on the FPGA for experimental results. FLC logic has used widespread in real-time applications. In [26-29], the authors introduced the implementations of FLC based on Field Programmable Gate Arrays(FPGA). Hardware-based solutions and software-based solutions are used for FLC applications. Hardware-based solutions are achieved at a high speed of inference, but they do not have flexibility because of some limitations. The main properties of software-based solutions have flexibility but have limitations rate [30]. The FPGA provided the solutions to overcome flexibility and speed limitations in the Hardware-based solutions and software-based, respectively [26, 30].The main objectives of the thesis are: To model the variable output voltage using the FLC simulation in the Matlab environment for the buck converter. Also the FIL co-simulation of the FLC and Verilog code for FLC. To implement the hardware of FLC using the FPGA board. To regulate and stabilize the main DC voltage bus under-voltage and load variations

The mathematical model of DC-DC buck converter, effects of constant power load on the buck converter, and its stability analysis using small-signal stability and the literature

reviewer of the previous compensation techniques of constant power load and their evaluation are given in the second chapter.

The third chapter presents the fuzzy logic control (FLC) as a new suggestion control for a DC-DC multi converter system with a constant power load. The complete design of the required system is explained. It also included the design of the PI controller. Additionally, the FPGA is used for designing and implementing the controllers in experimental and simulation approaches.

the fourth chapter includes in the discussion of the simulation and experimental results. To verify the designed control, the buck converter used as a source converter with fuzzy logic and PI controllers, which is feeding a mixture of constant power load, resistive load, and DC-DC buck converter. The design and validation of the overall system are achieved by using the Matlab/Simulink toolboxes, FIL tool, and experimental results.

Finally, conlcusion and future work are introduced in the fifth chapter.

2. CONSTANT POWER LOAD WITH BUCK CONVERTERS

2.1. Constant Power Loads

Constant power loads (CPL) means that the output power of the converter is constant, i.e., the output voltage drops when small variations occur in the current value (increasing current amount), which means that when neglecting the dissipated power into the circuit, the output power and input power are equal [17, 18]. The converter behaves as a CPL when it has closed-loop control and as a resistive load in open-loop as in Figure 2.1. [11, 31]. The power electronic converters tend to have CPL properties if them output voltage is bigger than voltage reference (V_c) [14, 18, 32-35]; in another word, the converter behaves as the resistive load at start-up but as a CPL when it exceeds the value of voltage reference (V_c) [35].

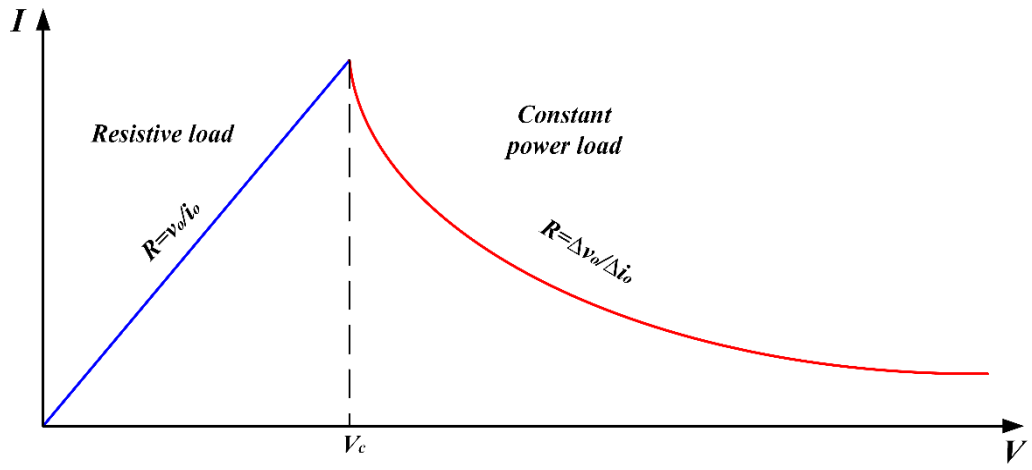


Figure 2.1. V–I curve of load converter

Many loads, like motor drives or electronic loads with tightly regulated controllers, behave as a constant power load [16-18]. Figure 2.2. is an example of CPL, that the motor is driving by DC-AC inverter. The inverter is tightly regulated to control the speed. When the load is rotating, the motor will have one to one of the torque-speed characteristics, and the relationship between the speed and torque is linear. For a linear relationship, each value of speed has only one corresponding amount of torque. Therefore, power equals the multiplication of torque and speed, which will be constant [16-18].

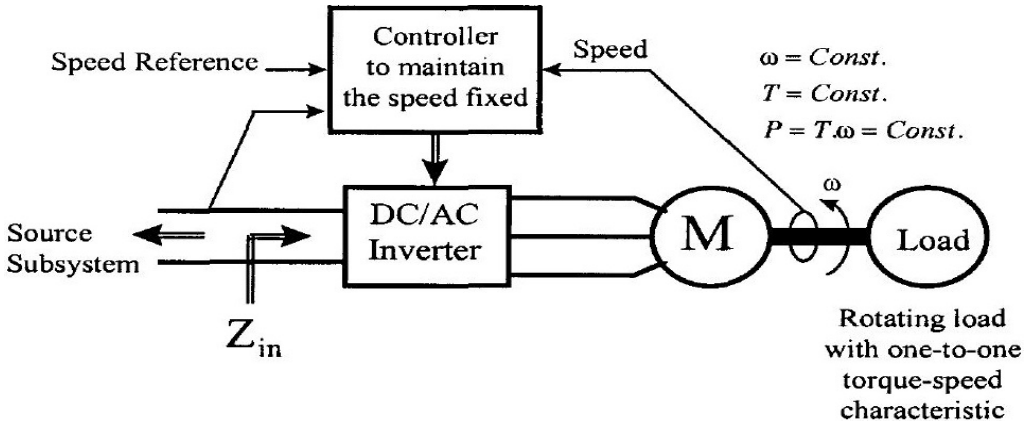


Figure 2.2. DC-AC inverter that presents a constant power load characteristic

Another example is a DC-DC converter, which feeds the electric load and is tightly controlled to maintain an output voltage fixed on the load [16-18], as shown in Figure 1.1. The power of the load is constant when there is a linear relationship between voltage and current.

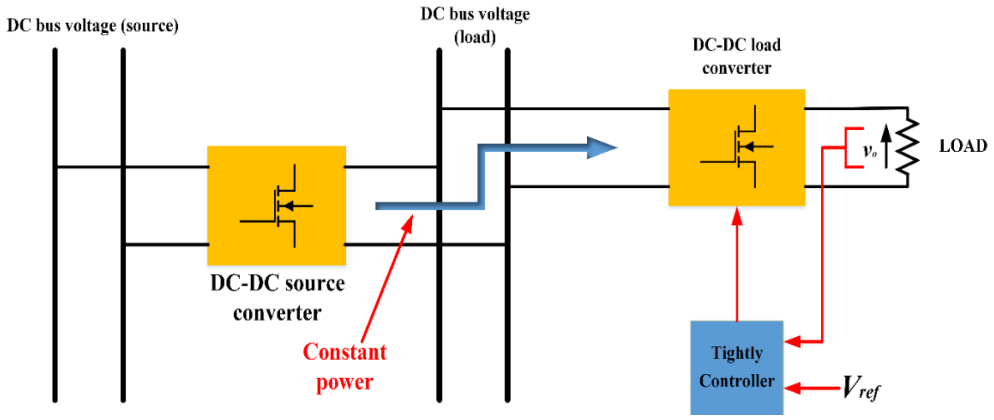


Figure 2.3. DC-DC converter with resistive load behaves as a CPL

In CPL, the output power will be equal to the input power, neglecting power losses in the system. As in [36], the mathematical model of CPL can be derived as follows:

$$P_{in} = P_{out} = constant \tag{2.1}$$

The differential change in the input power can be expressed as:

$$\delta P(v,i) = 0 = v\delta i + i\delta v \tag{2.2}$$

The input incremental resistance r_{in} can be defined as:

$$r_{in} = \frac{\delta v}{\delta i} = -\frac{v}{i} \tag{2.3}$$

The negative sign that appears in Equation (2.3) means that the CPL characteristics can be explained by the negative slope of the V−I curve shown in Figure 2.1 [37]. The CPL has inherent incremental negative resistance (INR). There is more than one way to realize a mathematical formula of INR [18]. This instability effect of NIR does not discuss when the converter is designed, but in a multi converter, the level should be taken into consideration. This phenomenon will impact the stability of the DC distributed power system and make the LC filter oscillatory [38].

2.1.1. CPL effects on the duty cycle

In a multiconverter (cascade converter [13]), the converters are connected in series (see Figure 2.3.). The first stage converter feeds the second stage converter with the desired voltage. For some reason, the input voltage of the second stage, i.e., the output voltage of the first stage converter, may be increased; the loop voltage control for load converter will reduce the duty cycle to regulate its output to the desired voltage. Hence, the current will also lower due to the reducing duty cycle. As a result, the increase in voltage led to a decrease in current and vice versa. This increasing or decreasing in voltage or currents introduce the instability effects on the main DC bus system and makes the system have low damping.

2.1.2. The incremental negative resistance (INR)

The converter that is used for open-loop or inadequate close loop control does not have constant power load properties. The CPL consumed a fixed power and Negative Incremental Resistance with its bandwidth control. In the CPL, the relative rate of change between the voltage and current is negative ($dv/di<0$), but the instantaneous value of impedance is positive ($V/I>0$) as shown in Figure 2.4 [14, 16-18, 33, 34, 39, 40]. The stability point of a system means; the system will return to a specific point if any disturbance occurs. The steady-state point in a system that includes the CPL is obtained when the CPL voltage is equal to the voltage source. At this point, the system will be stable. Nevertheless, if any disturbance occurs, the system cannot return to this point [41, 42].

This can be understood as follows: if a small disturbance makes the load voltage less than the voltage value of the stable point, then the load current will be bigger than the load current at a constant power of the load and result in the filter capacitor begins discharged. Thus, the load current will increase to make the power constant, and at the same time, the voltage will decrease. If a system does not have proper control to prevent this phenomenon during transient or any small disturbance, the voltage will be zero, and the current will go to infinity. Previously the system behaved as a feedforward. Now, if there are any changes in the voltage of the source converter (i.e., decreasing), the load converter will increase the duty cycle to regulate the voltage, which means the current will increase to maintain constant power [41].

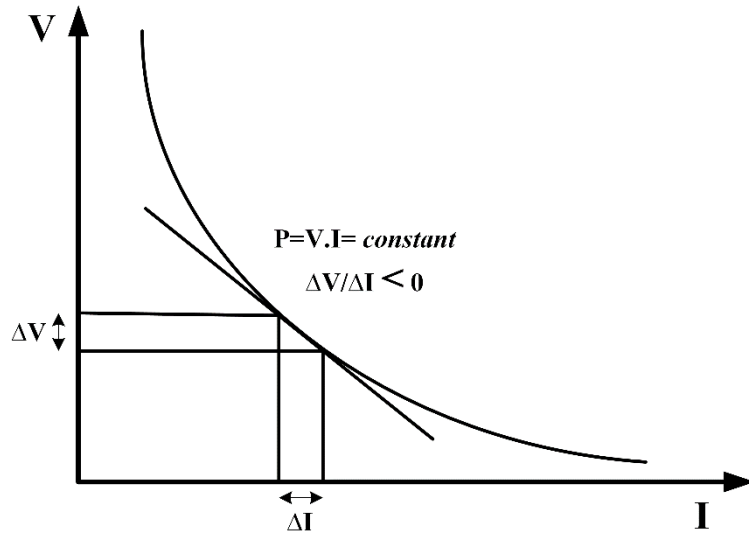


Figure 2.4. Negative impedance behavior of constant power loads

Figure 2.5. includes the connection of CPL with the parallel capacitor [22]; the state equation of the circuit can be written as follows:

$$v_c = \frac{P}{i} \tag{2.4}$$

$$-i_c = C\frac{dv_c}{dt} \tag{2.5}$$

The solution of these equations gives

$$v_c^2 = V_c^2 - 2\frac{P}{C}t \tag{2.6}$$

$$i = \frac{P}{\sqrt{V_c^2 + 2\frac{P}{C}t}} \tag{2.7}$$

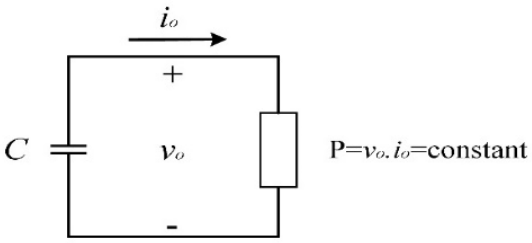


Figure 2.5. A constant power load parallels with a capacitor

The solved equations show the circuit that exists from the CPL and parallel capacitor is unstable because as ($t = V^2_C\, C/2P$), the voltage goes to zero, and the current goes to infinity. Therefore, the CPL is unpredictable with a parallel capacitor. The equilibrium point of the circuit is when the voltage of CPL is equal to the source voltage. In other cases, the system loses its stability and cannot restore the steady-state because the INR of CPL and voltage will go to infinity as the current goes to zero and vice versa, as shown in Figure 2.6.

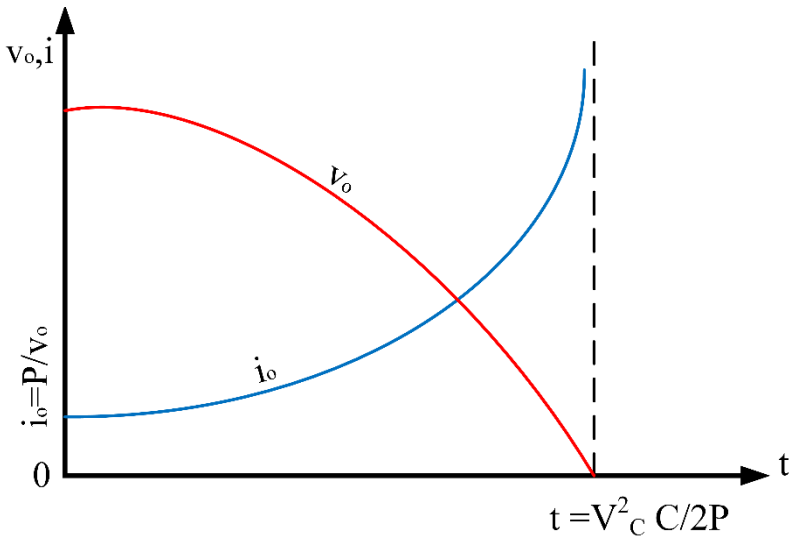


Figure 2.6. Voltage and current of the circuit shown in Figure 2.4.

2.1.3. Negative incremental resistance effects

As mentioned previously, a system that has a CPL could be unstable. This instability is produced by the interaction between the power system structure and the negative impedance created by the CPLs. Negative incremental impedance impacts the power quality of the system and can lead to system voltage oscillations or even collapse, and reduces system damping. These system voltage oscillations put additional stress on the components and may lead to the system failing or its components being damaged [21, 43].

Most often, a filter, which usually consists of the inductor (L) and capacitor (C), place after a pulse width modulation power converter to minimize the input current harmonics. Because of the small value of the resistance of the LC filter, a large transient oscillation can occur between *L*, *C* when operating conditions change suddenly [44].

CPL instability will occur when the applied control on a system is tightly regulated and has a closed-loop. Feedback controllers of the closed-loop depend on the process output (voltage or power). The NIR of CPL makes the damping of the input LC filter of the multiconverter system negative and the LC filter oscillatory [45]. Therefore, this oscillation at the output will make the system unstable. Thus, the instability effects of CPL (INR) can be summarised on any power electronic system as mentioned in [12, 43] as follows: CPL reduces the equivalent resistance of the system, causes a high inrush current as the voltage builds up slowly from its initial value, makes the system poorly dampened and impacts on the stability [15, 16, 39, 46, 47], which causes limit cycle oscillation in the DC bus voltage and currents and may lead to voltage collapse [21, 46, 48]

2.2. DC-DC Converters

The DC-DC converter is desired to convert the input DC voltage and current form to require the voltage and current form. The essential operation of the dc-dc converter similar to the ac transformer with a variable transform ratio and also uses to set up or down the output voltage. This converter has advantages like efficient power supplies, less size and weight, and more reliability and quality[49, 50]. Thus, they are widespread applications in spacecraft, modem aircraft, More Electric Ship (MES) power, International Space Station, submarine, etc. there are many functions of DC-DC converter can be similar as below:

1. Convert the input of DC voltage to a designed output voltage.
2. Isolate the supply side from the load or disturbing side.
3. Regulate output DC voltage under step change of load and line variation.
4. Reduce the ripple of output dc voltage.
5. Product the dc power system from electromagnetic interference

In general, there are many types of the DC-DC converter, but in this thesis is discussed the buck converter and boost converter. The IGBT and MOSFET power transistors usually use a converters structure. The output voltage of converters is determined by switching the power transistors, and its value deepened on the input DC voltage and on/off switching times [51] (see Figure 2.7.).

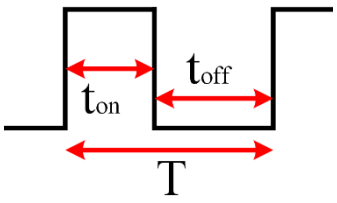


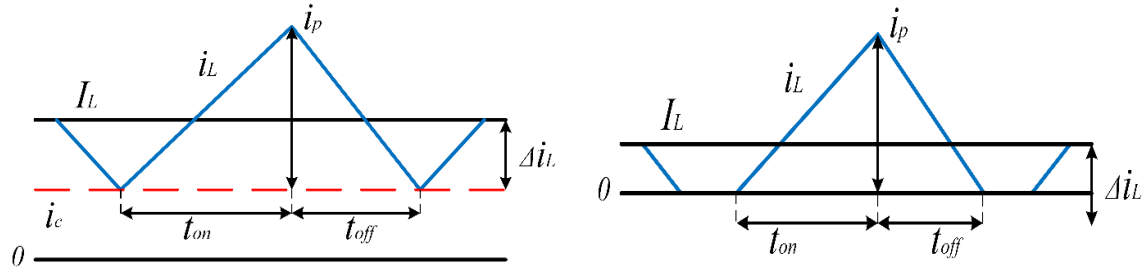
Figure 2.7. Switching times of IGBT

In other words, the output value calculates by setting the period of ON-time switching (t_{on}). This process is known as pulse width modulation (PWM) and the relationship between t_{on} to one cycle time (T) is the duty cycle (d) and described as below:

$$d = \frac{t_{on}}{T} = \frac{t_{on}}{t_{on} + t_{off}} \tag{2.8}$$

2.3. Stability Analysis for a DC-DC Buck Converter with CPL

The buck converter steps down the source voltage to the desired voltage. The buck converter can operate in two operation modes; Continuous Conduction Mode (CCM) and discontinuous Conduction Mode (DCM), as shown in Figure 2.8. Hence the CCM means the current inductor does not fall to, and the opposite is exact for DCM[50, 51].



(a) CCM (b) DCM

Figure 2.8. DC-DC buck converter operation modes

In this thesis, the stability analysis is introduced for CCM buck with constant power load. The stability analysis included the DC-DC buck converter with CPL using small-signal stability.

2.3.1. Small signal stability

DC-DC buck converter loaded by CPL

As known, the DC-DC buck converter has two switching times; ON and OFF periods. The described equations of ON period (see Figure 2.9.) is given below

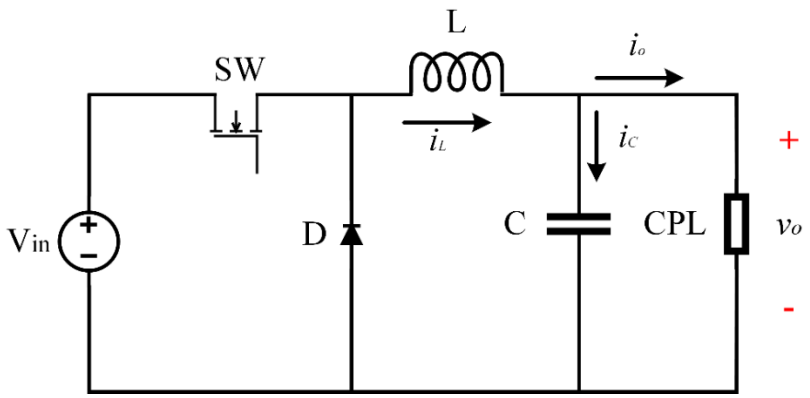


Figure 2.9. DC-DC buck converter with CPL

$$0 < t \leq dT \begin{cases} \frac{di_L}{dt} = \frac{1}{L}[dv_{in} - v_o] \\ \frac{dv_o}{dt} = \frac{1}{C}[i_L - \frac{P}{v_o}] \end{cases} \quad (2.9)$$

And for OFF period is described as:

$$dT < t \leq T \begin{cases} \frac{di_L}{dt} = \frac{1}{L}[-v_o] \\ \frac{dv_o}{dt} = \frac{1}{C}[i_L - \frac{P}{v_o}] \end{cases} \quad (2.10)$$

Equations (2.9) and (2.10) are nonlinear equations. A small disturbance in the duty cycle and the input voltage caused by small perturbations in the variable states is assumed [52].

$$\begin{aligned} v_{in} &= V_{in} + \tilde{v}_{in} \\ v_o &= V_o + \tilde{v}_o \\ d &= D + \tilde{d} \\ i_L &= I_L + \tilde{\imath}_L \end{aligned} \quad (2.11)$$

Where $\tilde{v}_{in}$ and $\tilde{d}$ are input variables and $\tilde{v}_o$ and $\tilde{\imath}_L$ are state-space variables and $\tilde{v}_o$ is the voltage output of the buck converter.

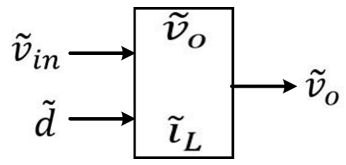


Figure 2.10. Inputs, state-space variables, and output of buck converter.

The small-signal stability is analyzed by determining the transfer function of the system and its pole locations on the frequency domain (S-plane) [53].

The system transfer function in the term $\tilde{v}_o$ and $\tilde{d}$ can be written as

$$H_d(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{\frac{V_{in}}{LC}}{s^2 - \left(\frac{P_{CPL}}{CV_o^2}\right)s + \left(\frac{1}{LC}\right)} \quad (2.12)$$

And in the term $\tilde{v}_o$ and $\tilde{v}_{in}$ can be written as

$$H_v(s) = \frac{\tilde{v}_o(s)}{\tilde{v}_{in}(s)} = \frac{\frac{D}{LC}}{s^2 - \left(\frac{P_{CPL}}{CV_o^2}\right)s + \left(\frac{1}{LC}\right)} \tag{2.13}$$

And the overall system is

$$\tilde{v}_o(s) = H_v(s) \cdot \tilde{v}_{in}(s) + H_d(s) \cdot \tilde{d}(s) \tag{2.14}$$

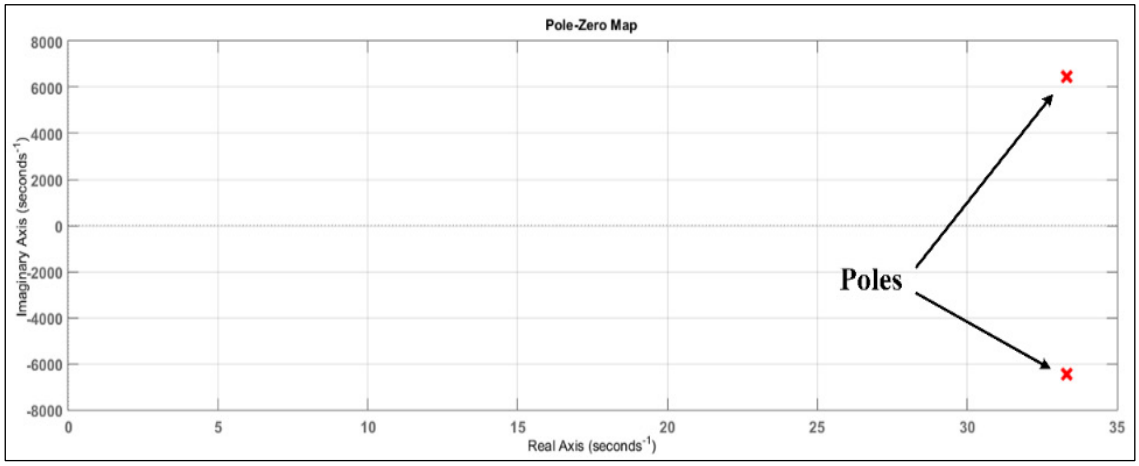


Figure 2.11. Pole positions

As seen from the equations (2.12), (2.13), and Figure 2.11. The DC-DC buck converter with CPL has two conjugate poles at (33.3 ± 6454.9j) lie on the right hand of S-plane then the system will be unstable. The parameters of system are L=1.6 mH, C=1000 mF, V_o=100 volt, D=50% and P_{CPL}=150 watt.

DC-DC buck converter loaded by CVL and CPL

Herein, the averaging modeling of DC-DC buck converter with resistive load and CPL load is discussed. Also, the resistive of the inductor is considered and its impacts on the system, as illustrated in Figure 2.12.

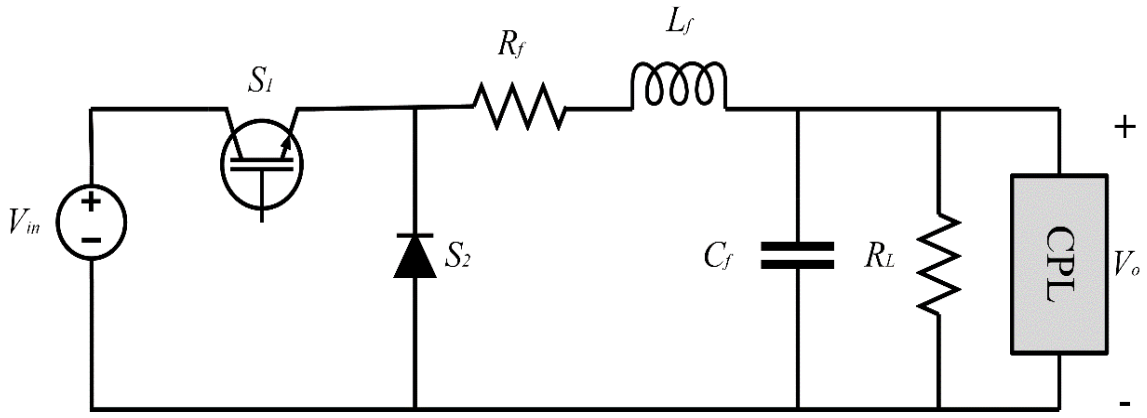


Figure 2.12. DC-DC buck converter fed resistive and CPL loads

The CPL can be modeled as the current source with a parallel resistor [20, 54], as shown in Figure 2.13.

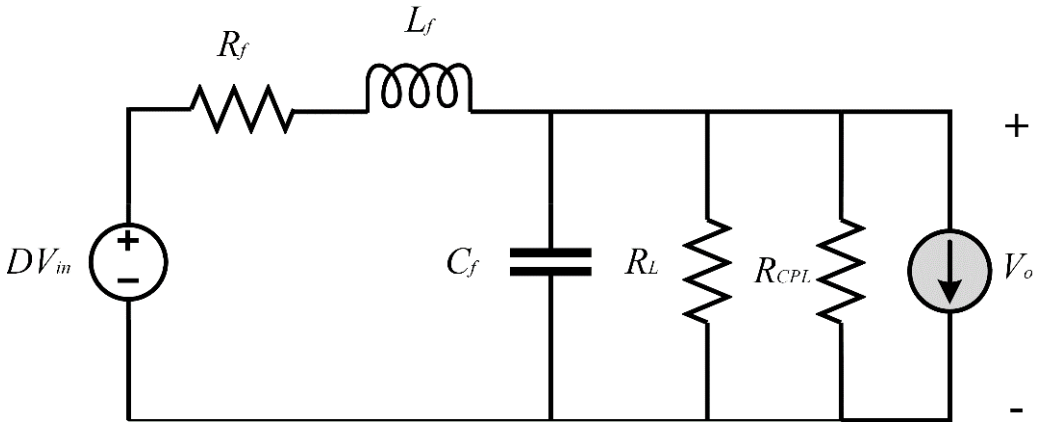


Figure 2.13.CPL load modeling in the power system

If R_{equ} is the equivalent resistance value of R_L and R_{CPL}

$$R_{equ} = R_L // R_{CPL} \tag{2.15}$$

Then, the described equation of the circuit in Figure 2.13. can be written as below:

$$\begin{aligned} L\frac{di_L}{dt} &= d \cdot V_{in} - v_o - i_L \cdot R_f \\ C\frac{dv_o}{dt} &= i_L - \frac{v_o}{R_{equ}} \end{aligned} \tag{2.16}$$

Then the transfer function of the circuit in S-plane can be written as below:

$$v_o = \frac{d(s) \cdot V_{in}}{LC \cdot s^2 + \left(\frac{L}{R_{equ}} + R_f\right) \cdot s + (1 + \frac{R_f}{R_{equ}})} \tag{2.17}$$

To determine the stability of the DC-DC buck converter, the poles of transfer function needed to calculate. DC in Figure 2.13. is do not have any effect on the LC filter damping or poles of filter [54]. The poles of the system have obtained as below:

$$p_1, p_2 = \frac{-\left(\frac{L}{R_{equ}} + R_f \cdot C\right) \pm \sqrt{(\frac{L}{R_{equ}} + R_f \cdot C)^2 - 4 \cdot L \cdot C \cdot (1 + \frac{R_f}{R_{equ}})}}{2 \cdot L \cdot C} \tag{2.18}$$

From equation (2.18) can be deduced as below:

First suggestion:

If R_{equ} has a negative value and its absolute value is smaller than filter resistance, the system has two poles in S-plane. One of the poles lies on the right-hand side of S-plane and another on the left side, and then the system is unstable.

Second suggestion:

If the criteria in equation (2.19) is satisfied then the system has two conjugate poles, and the real part value depended on $((L/R_{equ})+R_fC)$

$$\text{If } |R_{equ}| > R_L \quad \text{and } ((\frac{L}{R_{equ}} + R_f \cdot C)^2 - 4 \cdot L \cdot C \cdot (1 + \frac{R_f}{R_{equ}})) < 0 \tag{2.19}$$

Third suggestion:

$$\text{If } |R_{equ}| > R_L \quad \text{and } ((\frac{L}{R_{equ}} + R_f \cdot C)^2 - 4 \cdot L \cdot C \cdot (1 + \frac{R_f}{R_{equ}})) > 0 \tag{2.20}$$

Then

$$\left|\frac{L}{R_{equ}} + R_f \cdot C\right| > \sqrt{(\frac{L}{R_{equ}} + R_f \cdot C)^2 - 4 \cdot L \cdot C \cdot (1 + \frac{R_f}{R_{equ}})} \quad (2.21)$$

Then the system also has two conjugate poles, and the real part value depended on $((L/R_{equ})+R_f C)$.

Practically the absolute value of equivalent resistor R_{equ} is larger than the resistor filter value. The equation (2.21) is considered stable if the amount of $((L/R_{equ})+R_f C)$ has a positive sign. In another hand, if the value of equivalent resistor R_{equ} is negative, then the stability criteria become

$$\frac{L}{|R_{equ}|} < R_f \cdot C \quad (2.22)$$

From equation (2.22) to make the system stable, they needed to change the parameters of the system. The parameter changing led to a decrease in the efficiency of the system, as discussed in chapter 1.

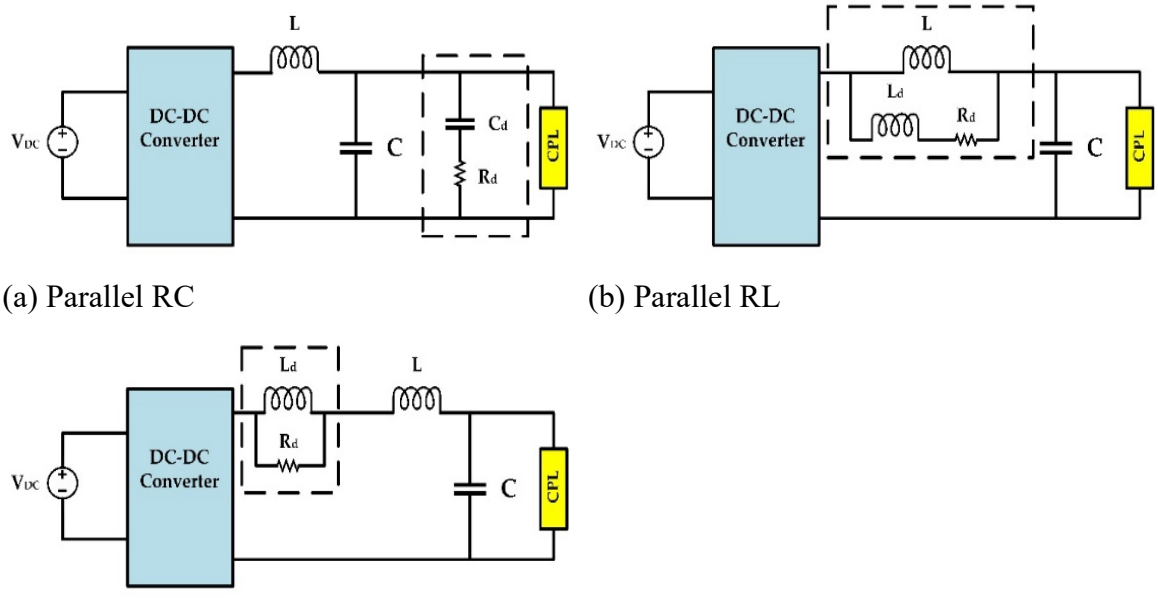
2.4. Compensation Techniques of The Instability of CPL

Because of the non-linearity and time dependency of converters' operation and the incremental negative impedance effects of constant power loads, classical linear control methods (like a conventional proportional-integral PI controller) have stability limitations around the operating points and do not apply to these systems. Therefore, digital and nonlinear stabilizing control methods must be used to ensure large-signal stability [14, 17, 18, 33, 40, 55, 56]. Compensation Techniques of the instability of CPL can be achieved by adding an extra element like passive elements or devices to the power system or redesigned the control loop of a source or load converter [43, 57].

2.4.1. Passive damping

Passive damping is a simple method to increase the damping of a system by adding passive elements; which contain resistance (R), inductor (L) and capacitor (C), to the input filter of the system, as described in [19, 58]. The authors introduced three methods for passive damping by adding *RC* and *RL* in parallel with the input filter and *RL* in series. In [59], the technique used is adding the only R in parallel with the L-filter. As in [58], the method proposed here to stabilize the system is a minimization of the peak output impedance of the filter by adding a passive damping (passive elements) circuit to the LC filter. The stability of the CPL system requires the impedance ratio Z_d/Z_1 to meet the Nyquist stability criterion, or the characteristic polynomial of $(1/(1 + Z_d/Z_1))$ to meet the Routh–Hurwitz criterion. The paper introduced three methods of passive damping, as shown in Figure 2.14:

1. *RC* parallel damping;
2. *RL* parallel damping;
3. *RL* series damping.



(a) Parallel RC

(b) Parallel RL

(c) Series RL

Figure 2.14. Proposed passive damping methods

These methods were tested by the authors, who obtained the following results: the best approach is adding RC parallel damping because significant CPL compensation by RL

parallel damping is needed to minimize the L-filter, which is undesirable. RL series damping can compensate if and only if R_{CPL} satisfied the criteria in equation (2.23), and the average dissipated power is the biggest in RL series damping and RC parallel damping and the smallest in RL parallel damping.

$$R_{CPL} > \sqrt[2]{\frac{3L}{2C}} \tag{2.23}$$

This method is simple to implement. It does not require the addition of any control terms to the control loop of the system. By using this method, the stability of the system is achieved. The efficiency of the system is decreased because there will be a more significant power loss when using this method. It will be expensive when passive elements are added, especially capacitors. This method in [19, 58] is valid for small disturbances [59].

2.4.2. Active damping

Active damping, another solution to the instability problem introduced by INR, involves a modification control loop by creating a damping effect of passive damping or modifying the DC bus capacitance. Also, it can be achieved by adding a device that injects a compensating current [20]. The active damping can be done by three methods [12]. The first is source-side active damping. The compensation at the source subsystem by active damping aims to add a loop in loop control to improve the output impedance of the feeder converter to satisfy the impedance stability criterion. This type is impossible to apply to a system when the input stage is LC or uncontrolled rectifiers. To overcome the instability effect of INR, the CPL side Active Damping is considered when the source subsystem of a CPL is the LC filter. The concept of this method is achieved by injecting a current or power into the CPL control loops to modify the input impedance Z_{in}, such that Middlebrook's stability criteria are satisfied [12, 43]. The third is adding an auxiliary device that injects the desired compensating current within an operation range system.

Virtual impedance or resistance is one method of active damping introduced by researchers in [8, 20, 37, 47, 60-64]. Active damping means adding virtual resistance to the control loop achieves the improvement transfer function of a system and forces the movement of the poles

towards a stable region (left half of s-plane). It guarantees that any extra power does not dissipate into the system [20, 37, 60], as in Figure 2.16. In fact, the virtual resistance makes the output impedance of the source converter less than its maximum value [57]. The output voltage V is measured and controlled to track the reference voltage as in equation (2.24) instead of a constant voltage reference, as shown in Figure 2.16.

$$V_{ref1} = V_{ref} - iR_{eq} \tag{2.24}$$

The new reference value will vary according to the value of the load current and hence produces the equivalent function of adding physical resistor R_{eq}. [37, 60]. In [20], the authors presented a new method to overcome the problems of CPL by adding virtual resistance, which will affect the series resistance with an inductor to the feedback control system. In [8], the authors introduced the virtual impedance as series-connected resistance and inductance and two types of the stabilizer; one is based on capacitor voltage feedback, and the other is based on inductance current feedback for achieving a virtual impedance method and a model including a droop control index. In [62], an additional proportional voltage feedback control is inserted with virtual resistance to improve the system performance and overcome the disadvantages which produced from adding a large value of virtual resistance. One of these advantages is the region stability of virtual resistance will narrow as the output power increases [12].

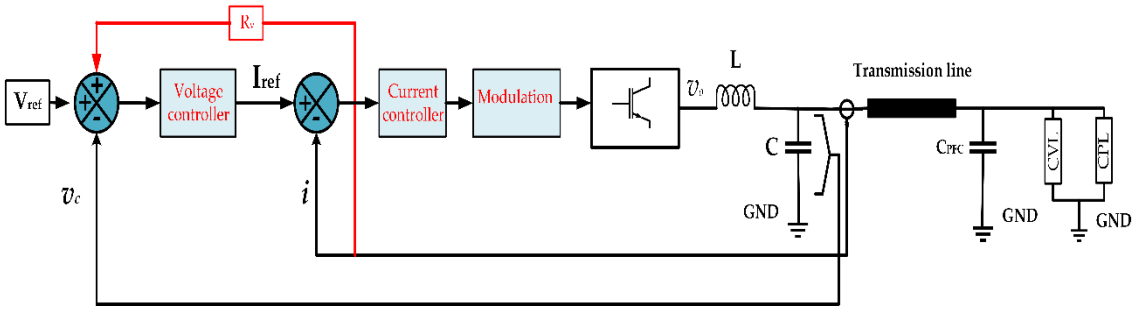


Figure 2.15.Active damping using virtual resistance

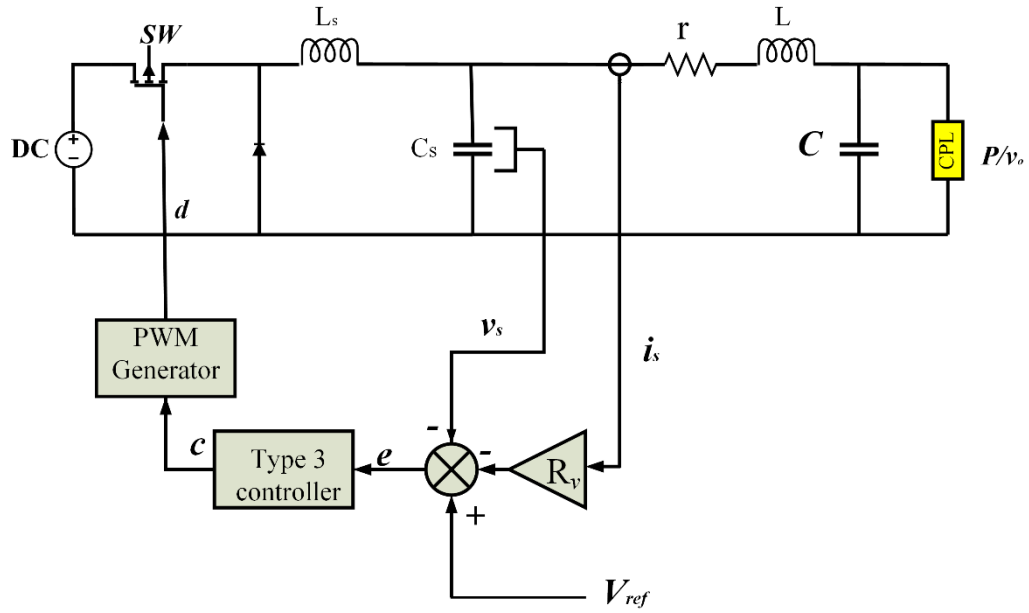


Figure 2.16. Active damping using virtual resistance and Type 3 controller

In [65], a feed-forward control with extra elements to improve the stability of hybrid electric vehicles (HEV) with CPL is introduced. The purpose of this method is changing the impedance of the load converter to match the impedance of the source. The changes are approved by the impedance frequency and analyzed by a low pass filter, and negative impedance can be eliminated by adjusting the virtual resistance in the control loop. In [66], active damping was achieved by modifying the duty ratio of the converter by using a first-order high-pass filter with a corner frequency and high magnitude.

In [67, 68], the authors presented an input-resistance compensator to eliminate the instability of INR in a system that has a power electric brushless DC motor drive with constant power-load characteristics, as shown in Figure 2.17. The strategy is to feed a portion of the changes in the DC-link voltage into the current control loop to modify the system input impedance in the mid-frequency range and thereby to damp the input filter. The input-resistance compensator is a high-pass filter with corner frequency and high-frequency magnitude. Its operation depends on the DC link voltage. The current output is a current (the stabilizing signal) that will act with the speed control loop to give a current reference to the control motor current by high-frequency PWM with a duty cycle determined by the PI controller. At a steady-state, the authors assumed the output of IRC would be zero if there is a change in the DC link voltage, but if the output of IRC is non-zero, then a signal will be generated to modify the motor current and the inverter input impedance, damp the DC-link oscillations.

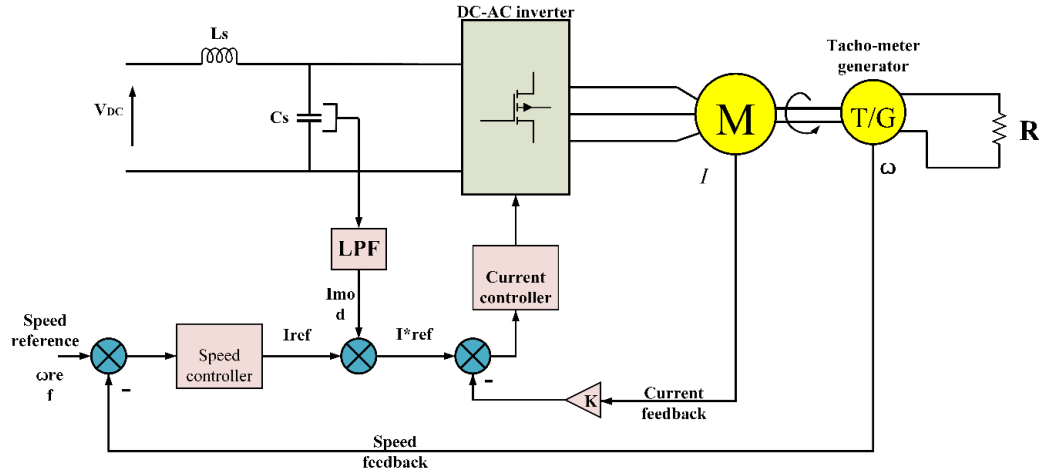


Figure 2.17. The input-resistance compensator (IRC)

In [21], a new device called a solid-state defender (SSD) is added between the load converter and source to protect the system and its elements against the fault and instability phenomena of INR and prevent the system from failure or damage of components. The SSD works as a power buffer in the bus fault case and transfers the stored energy in a capacitor to feed the load and current limiting in load fault by limiting the output current. On the other hand, it works as an impedance transformer to address the oscillation and transience produced by INR. The SSD improves the power quality of the system and eliminates the oscillations caused by the negative incremental impedance characteristic of loads. Active damping has received interest from researchers [8, 20, 37, 47, 57, 60-64, 69]; however, active damping causes effective performance but only compensates for limited values of CPL [43] and sometimes causes the output voltage to drop, as in [20].

2.4.3. Space pole placement control

The Space Pole Placement Control is used to shift the pole of the system from RHP to LHP of the s-plane. A new pole location must be chosen to satisfy the characteristic equation of the closed-loop system to make the system is stable. According to the paper, this method can be achieved by multiplying the specific gain (calculated by Ackermann's formula) by the state variables (inductor current and voltage capacitor) in closed-loop control. However, the result is subtracting from the reference voltage. The generated switch pulse has been produced from a comparison of the difference with the tooth signal, as shown in Figure 2.18 [41]. This method needs to represent all the state variables in a control loop [12, 41].

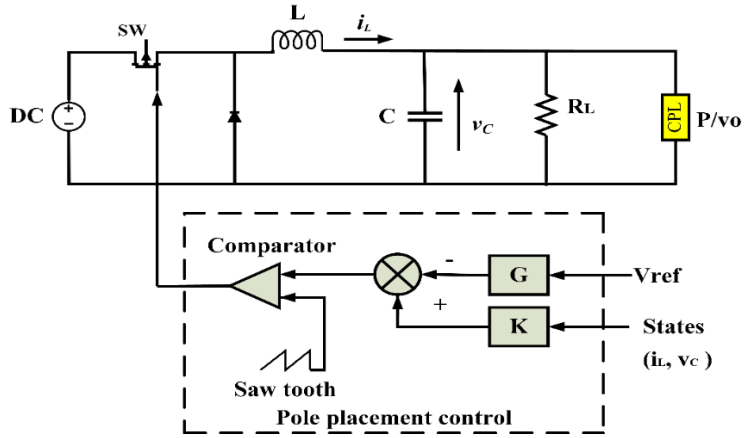


Figure 2.18. The space pole placement control

2.4.4. Pulse adjustment control technique

The papers [34, 40, 55, 70] presented the pulse adjustment control technique as a new control method to damp the instability caused by CPL with a DC-DC converter in vehicular systems. The pulse adjustment control is a digital control that drives the PWM control. The adjustment controller regulates the output voltage by generating high and low power pulse by comparing the output voltage and reference (desired) voltage and sending this pulse to the PWM. For output voltage (capacitor voltage) less than the reference voltage, the controller will increase the transferred energy from input to output. The CPL will consume the required energy, and voltage will be increased as a result of charging the capacitor with the remaining power, as in Figure 2.19. This paper presented the same controller as in [40] to provide the buck-boost converter but in discontinuous conduction mode (DCM). The drawbacks of this technique are high output voltage ripple, noise, and the sub-harmonic presented at the output voltage, although it has fast response times and a robust controller [71].

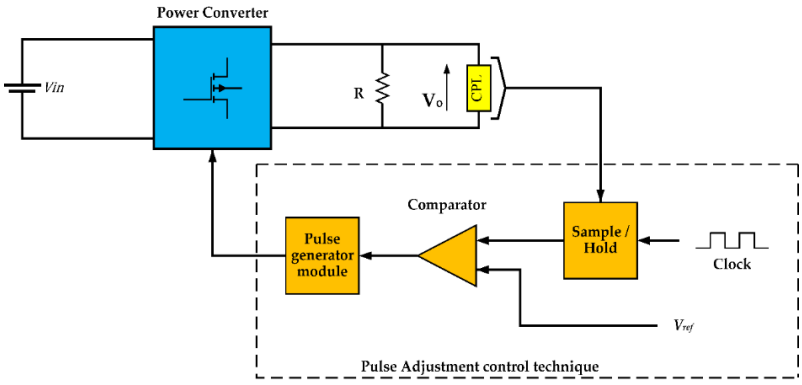


Figure 2.19. Pulse adjustment control technique

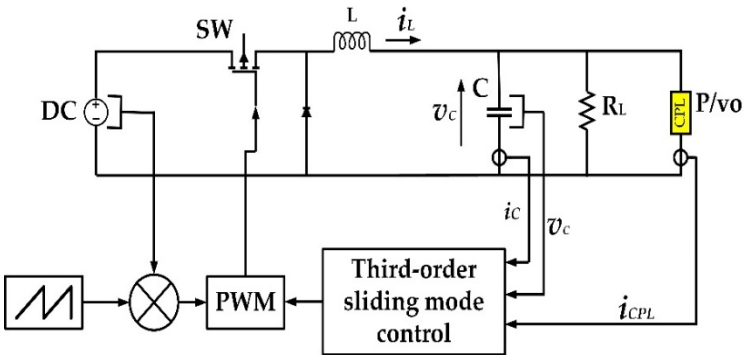
2.4.5. Sliding mode control

Sliding mode control has been used to address the instability effects of INR in the literature [14, 17, 43, 56, 72-78]. The aim of this controller is to control the output power of a DC-DC converter with CPL by setting the reference value of power and comparing it with the measured output power of the DC-DC converter [14, 17]. The proposed sliding mode control outputs a duty ratio, which is used to generate pulse-width modulated (PWM) gate signals for the DC-DC converter.

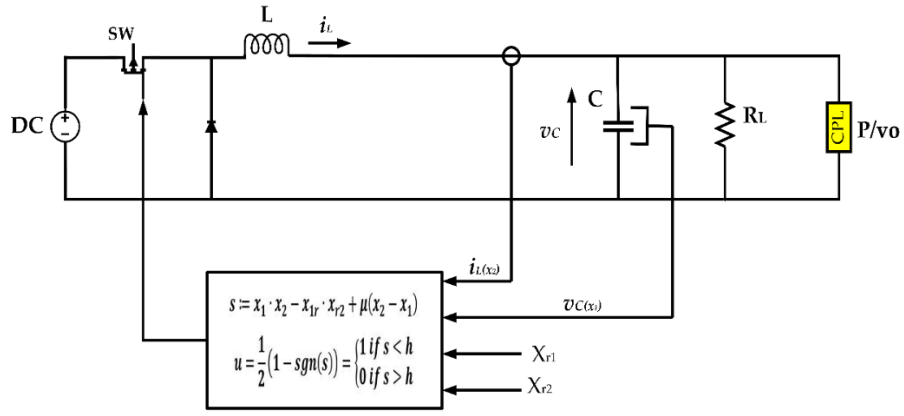
This controller improves signal stability and dynamic response; however, it is sensitive to significant changes in load [17], and the controller is capable at a high voltage above 400 volts but has disturbance at low voltages [56], which means the output voltage is not fixed. In [17], the authors tested the CPL with a parallel capacitor by using a series inductor and a buck converter. The circuit is unstable: instability will quickly appear in the buck converter, and other instability will occur within a short time. Due to the instability of CPL that occurs within an interval smaller than the switching time, there is a need to increase the switching frequency of *L* and *C*. The paper presented the sliding mode as improving the large signal stability and dynamic response of the buck converter. The objective of the control system in DC-DC converters with constant power loads is to control the output power. P_{out} is the output power, and *K* is the output power reference.

In [56], a third-order SMC is applied to control the buck converter. The single triangle is regulated by the input voltage to use with SMC output to generate a single control to drive the converter, as in Figure 2.20a.

In [73], the stable sliding surface (s), shown in Figure 2.20b, is designed to obtain system control law (u) is to meet the system stability requirements with reference values for the inductor current and capacitor voltage.



(a)



(b)

Figure 2.20. Sliding mode control with CPL

2.4.6. Model predictive control

In the literature [44, 48, 79, 80], researchers introduced a model predictive control as a solution to mitigate the instability caused by CPL. In [80], a power buffer interfaces between the source converter and CPL to modify the load impedance of during a transient or fault case. The model predictive controller (MPC) controls the variation of the DC link voltage and adjusts the load impedance, which is seen at the point of common coupling. In [44], MPC is used with hybrid energy storage to manipulate the energy flows between the generator, load, and a hybrid ES, which is shown in Figure 2.21. In [44, 80], the MPC is not utilized directly to compensate the instability effects of CPL, but in [80] there is introduced an optimal trade-off between modification of load impedance, variation of DC-link voltage and battery current ripples; in [44] This is used to design and/or specify the requirements for the ES to achieve the desired transient response. The required duty cycle of the converter is calculated based on MPC strategies to mitigate the instability induced by CPL. The duty

cycle configurations are chosen to guarantee the stabilization of the CPL by associating the CPL current and voltage with the predicted output voltage values of the converter [48].

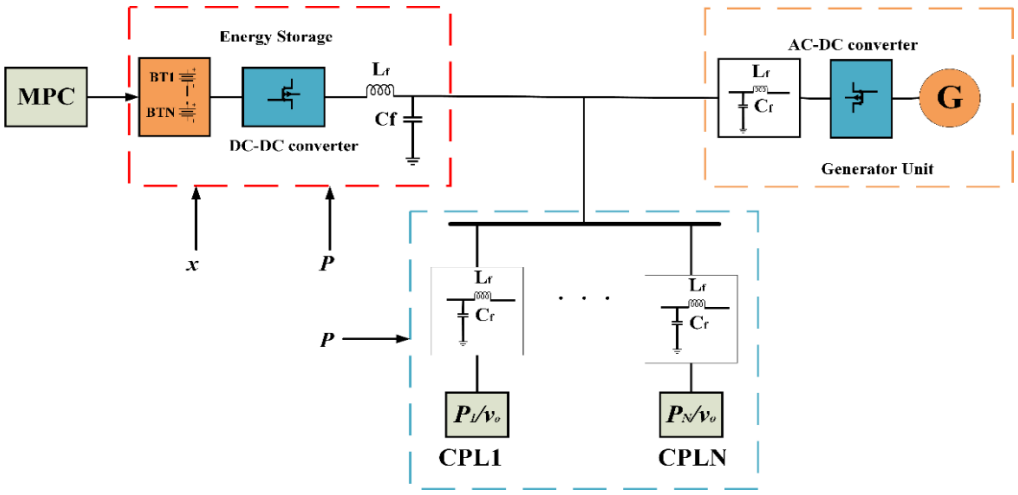


Figure 2.21. Model predictive control

2.4.7. Feedback linearization

Feedback linearization is a nonlinear control technique to overcome the instability caused by CPL, as proposed in [39, 45, 81-83]. This technique aims to cancel the nonlinearity introduced by CPL by determining the parameters that can be manipulated to obtain a system without instability without using a conventional PI controller, which has its disadvantages. In [39], the authors discuss the stability of a DC-DC buck converter that is feeding the resistive load (constant voltage load (CVL)) and CPL, the large-signal stability used, and the stability of system tested by Lyapunov theory.

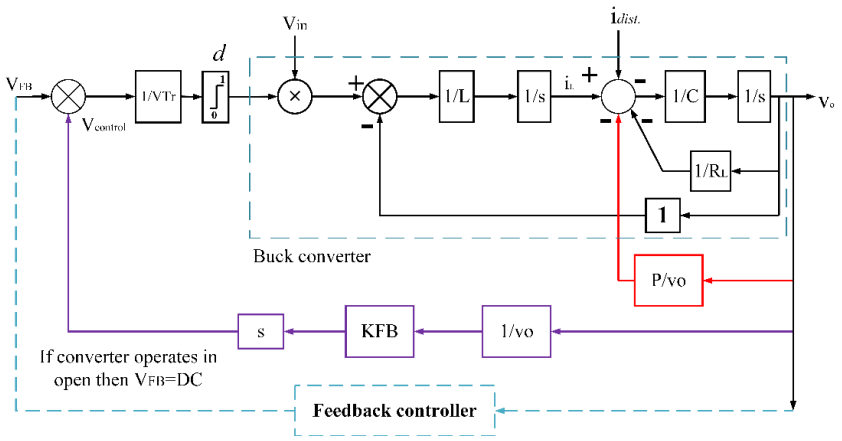


Figure 2.22. Feedback linearization of the buck converter

3. DESIGN AND IMPLEMENTATION OF THE SYSTEM

3.1. Fuzzy Logic

The fuzzy logic is an intelligent and nonlinear controller which its concept was introduced by Lotfi Zadeh, a professor at the University of California at Berkley [18]. FLC is not needed an exact mathematical model like other control methodologies [18]; it requires an understanding of the system, which is to controlled [19, 20]. According to [19], fuzzy control has the best performance among other controllers in the DC-DC converter.

The FLC is proper for complicated and extensive power system because it has advantages as: is not need accurate mathematical models. Therefore for an expanded system is useful when the mathematical model becomes difficult to modeling. FLC is depended on deduction so able to incorporate human intuition and experience.

Besides, the FLC is robust against variations of the parameter with time [14, 17]. With the increasing deployment of microgrids and smart grids, constant power loads are increasing gradually [18-24].

The fuzzy logic control is introduced as a new compensation method to cancel or mitigate the instability effects of constant power load. The fuzzy logic control (FLC) is proposed to overcome the nonlinearity and variation of a system. Structure of fuzzy logic

3.2. Fuzzy Logic Controller

The principal elements of a typical fuzzy logic controller are shown in Figure 3.1. These elements are described in [23] as the Fuzzification module (fuzzifier), Knowledgebase that includes the rule base and database, the Inference engine, and the Defuzzification module (defuzzifier).

Fuzzification

In this step, classification and transformation of crisp input data into desired linguistic values or sets are done. The fuzzification is the first stage in fuzzy logic and means to convert real values to variables that are defined in a limited number of membership functions. The conversion of a large number to small and limited quantities in a specific domain has an advantage. The advantage is the number of values that are requiring to process, will reduce. This means the data processing operation will perform faster computation.

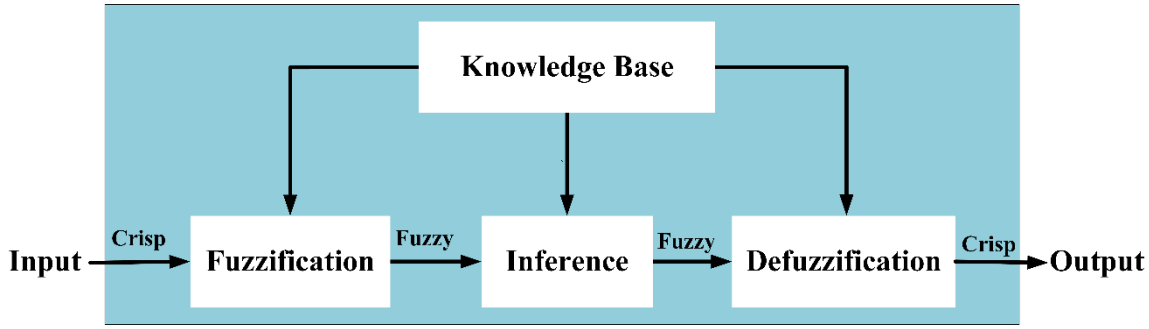


Figure 3.1. Principal elements of a typical fuzzy logic

Knowledgebase

The knowledge base has basic definitions for fuzzification processing, membership functions control rules, parameters, and database of fuzzy logic control. The knowledge base consists of two-part the rule base and database.

The database has the needed data of the system.it is provided the essential definitions for fuzzification processing like as the representation of fuzzy sets for input and output variables, the membership functions information, and the mapping processing between the fuzzy and physical domain.

The base rules, also known as fuzzy rules, of fuzzy logic, is not deepened on a mathematical model like as on another controller. They write in the form of IF . . . . THEN statements. The rules are depended on the fuzzy inference understanding, and the conditions and output are associated with linguistic variables. For example:

IF e is Negative Big condition statement
THEN U is Positive Big conclusion statement

The input (e) and the output (U) are fuzzy variables (linguistic variables), while Negative Big and Positive Big are the linguistic values.

Inference engine

The inference engine is also named decision-making logic . in decision making logic, the decision processing is executed. It represents the core of the FLC. It can stimulate human intuition and experience [23-25]. The inference engine implementation is done by using fuzzy reasoning methods. Herein is discussed mostly common used minimum product maximum method that is most commonly used in many applications.

Minimum product maximum

If there are two fuzzy rules, they can be written as follow

$$\begin{aligned} &\textit{Rule 1: if } x_1 \textit{ is } A_1 \textit{ and } x_2 \textit{ is } B_1 \textit{ then y is } C_1 \\ &\textit{Rule 2: if } x_1 \textit{ is } A_2 \textit{ and } x_2 \textit{ is } B_2 \textit{ then y is } C_2 \end{aligned} \tag{3.1}$$

Let assume the X_1 and X_2 are a real number that is gotten by x_1 and x_2

$$\begin{aligned} f_1 &= U_{A_1}(X_1) \times U_{B_1}(X_2) \\ f_2 &= U_{A_2}(X_1) \times U_{B_2}(X_2) \end{aligned} \tag{3.2}$$

C_{A1}, C_{A2} are outputs of fuzzy sets that represent the control rule and their action. C_{A1}, C_{A2} cab be calculated as

$$\begin{aligned} C_{A1} &= f_1 \wedge C_1(y_1) \\ C_{A2} &= f_2 \wedge C_2(y_2) \end{aligned} \tag{3.3}$$

Where $\wedge$ is minimum operation. however, the output membership can be determined as

$$U_c = C_{A1}(y_1) \cup C_{A1}(y_2) \tag{3.4}$$

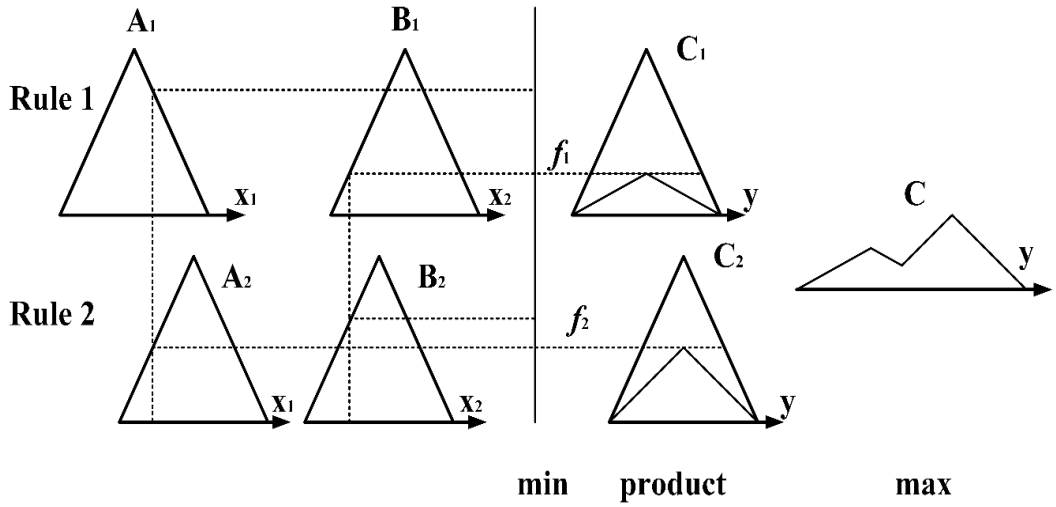


Figure 3.2. Minimum product maximum method

Defuzzification

In the defuzzification process, the output linguistic values concluded by fuzzy rules are converted into a crisp value. The purpose is to determine the one crisp value that best illustrates the calculated fuzzy values of the linguistic values. The output defuzzification represents the objective that requires to control a system. However, there are different mothed to do this processing, but the commonly used are:

1. Center-of-Maximum
2. Mean-of-Maximum
3. Center of Gravity

The center of gravity has discussed the method in this thesis, and its concept will explain in section 3.2.1. defuzzifier.

3.2.1. Design processing of the fuzzy logic controller

In general, the design steps of a fuzzy logic controller can be divided into four stages, which are explained as follows:

Membership function

The variables of the fuzzy logic controller consist of inputs and outputs. The number of variables deepened on the design system. The universe of discourse of these variables belongs to real number axes and have small intervals determined between x_{min} and x_{max}. A universe of discourse of one fuzzy variable can be divided into overlapping sets and called fuzzy sets or linguistic variables as standard. The odd number is be assigned of these sets, and the number of rules is depended on their numbers. However, the fuzzy set is called a membership function. The membership function is mapped the crisp amount into a fuzzy amount.

There are many shapes of membership functions that are included Γ-function, S function, *L*-function, triangle function, trapezoidal function, etc.…., but the most commonly used are Γ-function, *L*-function and triangle function as shown in Figure 3.3.

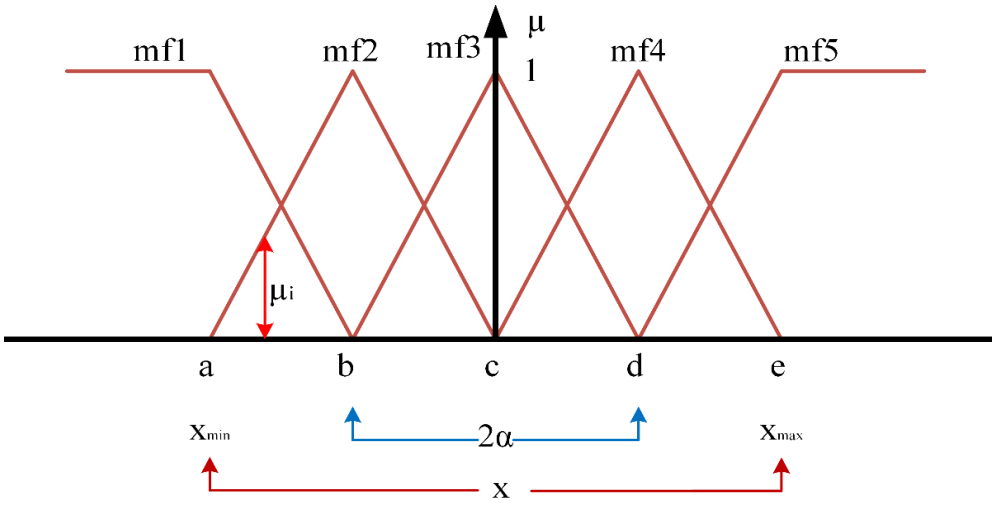


Figure 3.3. Membership functions

From Figure 3.3, the membership function (mf2, mf3, and mf4) are asymmetrical and overlap to another membership function by 50%. The chosen shape of membership is triangular and the described equation on (3.5)

$$f_i(x) = \begin{cases} \dfrac{x - \mu_i + \alpha_i}{\alpha_i}, & \mu_i - \alpha_i \le x \le \mu_i \\ -\dfrac{x - \mu_i - \alpha_i}{\alpha_i}, & \mu_i \le x \le \mu_i + \alpha_i \end{cases} \tag{3.5}$$

Where the i-th sampling instant is used as inputs of fuzzy controller, μ is the centroid of the i-th membership function, and α is a constant that determines the spread of the i-th membership function.

The variables of any membership for triangular function (mf2) α_i and μ_i can be determined as:

$$\alpha_i = \frac{x_{rangi}}{n - 1} \tag{3.6}$$

$$\mu_i = \begin{cases} 0, & x > c \text{ or } x < a \\ \dfrac{x - a}{b - a}, & a < x \le b \\ \dfrac{e - x}{b - c}, & b < x \le c \end{cases} \tag{3.7}$$

Where i=1⋯n, n is the linguistic variables number's and x_{rangi} is described as

$$x_{rangi} = x_{maxi} - x_{mini} \tag{3.8}$$

The mf1 is *L*-function that described equation can be written as below

$$\mu_i = \begin{cases} 1, & x < a \\ \dfrac{x - b}{a - b}, & a < x \le b \\ 0, & x > b \end{cases} \tag{3.9}$$

The mf5 is *Γ*-function that described equation can be written as below

$$\mu_i = \begin{cases} 1, & x > e \\ \dfrac{x-d}{e-d}, & d < x \leq e \\ 0, & x < d \end{cases} \tag{3.10}$$

Fuzzy rules

The fuzzy rules are the relationship between the input and outputs of fuzzy sets. They commonly are found in the form [if A and B then C]. The A and B and are called rule antecedents, and C is Known as rule consequence. Each fuzzy rule describes a fuzzy patch in the state space system. The adjacent of a fuzzy rule characterizes the fuzzy input range in the state space. Therefore only one of state-space will enable that is to cover a definite number such fields. The structure is designed to set on fire all rule at the same moment. Therefore this makes more easy and fast VLSI and digital design.

Figure 3.4. Shows a fuzzy system with two inputs and one output, and the E_1 is mapped by inputs A_1 and B_1 by using the rule [if A_1 and B_1 then C_1]. Then the activated set of E is combined and assigned to a corresponding fuzzy set of C. the active of rule consequent is represent the minimum value of two antecedent values and is a scalar value.

$$C = \sum_{m}^{i} E_i \tag{3.11}$$

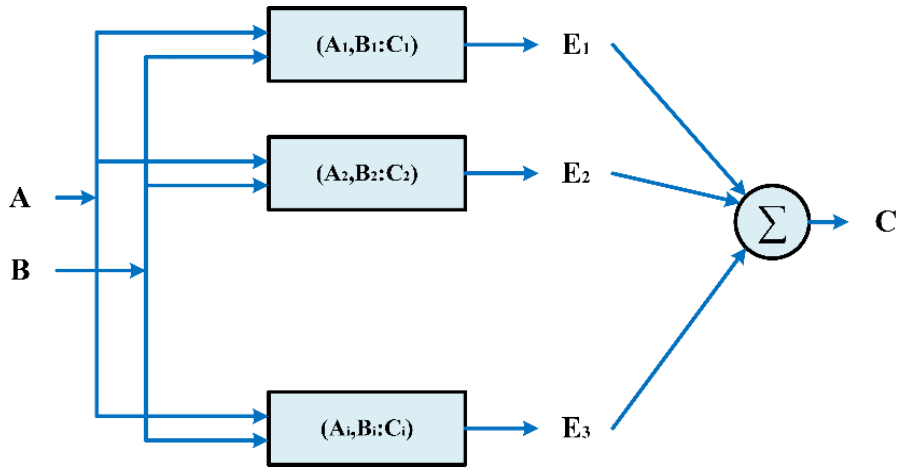


Figure 3.4. Fuzzy system

Mamdani model

Fuzzy inference processing is used the rule bases and alpha value to conclude the output of fuzzy logic. Different ways are used for achieving this process, but there are two types, the Mamdani and the TSK models.

This thesis will discuss the Mamdani model. In 1974, the Mamdani model concept was used for building the fuzzy system, Prof. Ebrahim Mamdani. It is applied to control a boiler combination and the steam engine. The basic idea of fuzzy rules is formulated by experienced human operators. However, the Mamdani model is widely used for fuzzy inference processing.

The Mamdani mostly uses the max-min or max-dot ways. These methods produce inferred results containing membership functions. The inference processing has two steps: the first step is deducing the output of every rule, and the second is aggregating the specific rule of fuzzy outputs to get the system output. It assumed that there are K rules and j-th rule can be written as below

$$\text{IF } e_1 \text{ is } a_{j1} \text{ and } e_2 \text{ is } a_{j2} \dots e_n \text{ is } a_{jn} \text{ THEN y is } b_j \tag{3.12}$$

The j-th merge the alpha levels of total fuzzy variables by and-type aggregation

$$\partial_i = \wedge(a_{j1}(e_1), a_{j2}(e_2) \dots a_{jn}(e_n)) \quad (3.13)$$

The results combine with their consequence b_j to calculate the output of each rule. In the Mamdani processing, the fuzzy output prepares K_j is gotten by adding the above-deduced alpha levels.

$$\mu_i(y) = \partial_j \rightarrow b_j(y) \quad (3.14)$$

The aggregation of deduced outputs of rule the complete system $\mu(y)$ the inferred rules are aggregating by an or-aggregate.

$$\mu(y) = \vee \mu_i(y) \quad (3.15)$$

Defuzzifier

In this stage, the linguistic values are converted to crisp values. There are many tequinches to implement the conversion operation. The mostly used tequine is the Center of Gravity (COG) Method. The concept of center of gravity method has the same phasic formula of center gravity as shown in Figure 3.5, and it can be formulated as equation

$$COG = \frac{\sum_x \mu(x) \times x}{\sum_x \mu(x)} \quad (3.16)$$

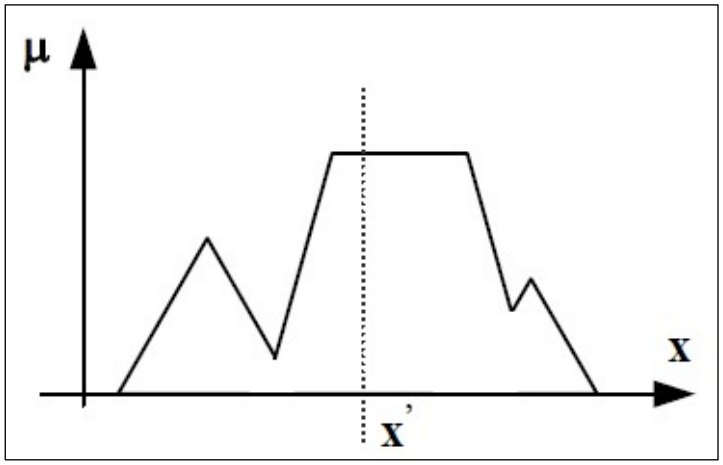


Figure 3.5. Center of gravity method

3.2.2. Fuzzy logic controller for DC-DC converter

In this thesis, the objective is to control the output voltage of buck converter, which is feeding CPL, load converter, and resistive load, based on a fuzzy logic controller, and by matching the reference value of voltage. In the FLC, the choice of controller inputs and outputs is dependent on the type of the controlled system and the required output. The most popular controller inputs are an error (e) and the rate of change of the output (e'). The output controller is a duty cycle to drive the buck converter, as shown in Figure 3.7.

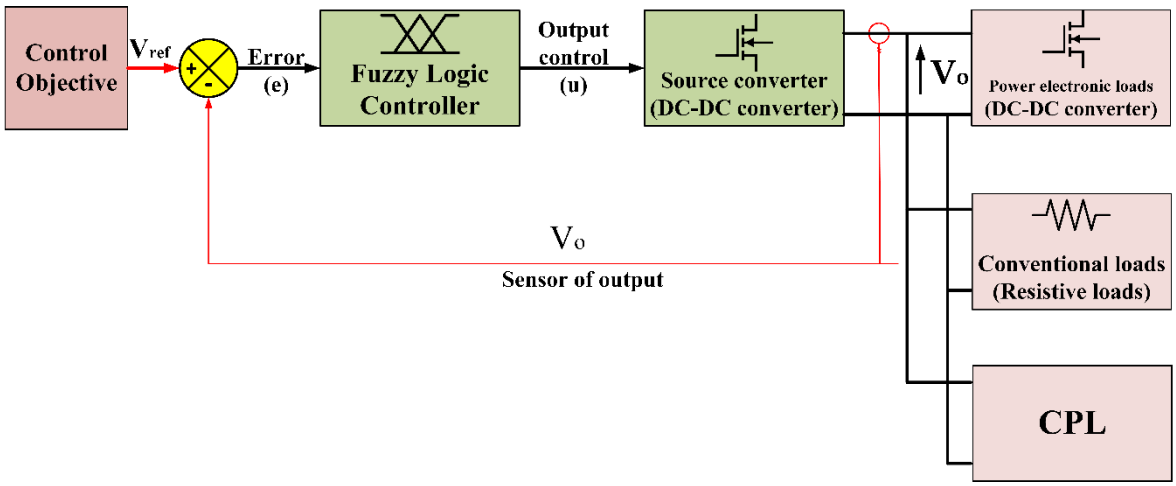


Figure 3.6. Overall proposed system

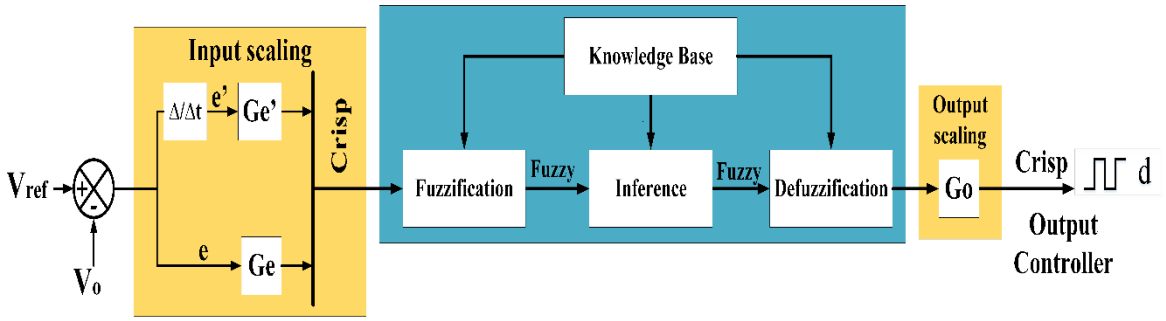


Figure 3.7. Fuzzy logic controller

The error and variation of error can be written as:

$$e(n) = V_{ref} - V_{meas(n)} \tag{3.17}$$

$$e' = e(n) - e(n-1) \tag{3.18}$$

It is evident from Figure 3.7 that the fuzzy logic consists of four elements as following: fuzzifier that converts input data from crisp to proper fuzzy values in fuzzy sets. The input data in control system applications can be obtained from the sensor (in this project, voltage sensor LV-25p). The outputs data of the sensor transform to corresponding fuzzy values in membership functions that are set up as fuzzy sets.

The membership functions draw crisp values into fuzzy values. A set of membership functions are defined for five linguistic variables: NB, NS, ZZ, PS, and PB, which stand for Negative Big, Negative Small, Zero, Positive Small, and Positive Big, respectively, as shown in Figure 3.8 [84]. Many shapes can be represented by memberships function. The triangle membership is used for the proposed controller in this thesis and can be described in equation Knowledgebase which has two sections - the database which contains the linguistic definitions, and the rule base which has a significant role in fuzzy logic control. However, the fuzzy rules are written in the form of (IF . . . . THEN) statements as below:

IF error (e) is A and e' is B rule antecedent
THEN output (u) is Ui rule consequent

Another part of the system is an inference engine. In this block, decision making is done. Then there is the defuzzifier, which converts the FLC deduced control actions from fuzzy values to crisp values[85].

The defuzzification process is represented the final process of fuzzy logic that resolves the crisp values output by determining the deduced rules into one output value. The method of defuzzification is used the physical concept of the center of gravity. The calculation of the crisp output, the utilized technique determines the weighted average of input membership values and the center point of each of the fuzzy output set. In this method, the output membership function should be symmetrical according to the center value. Input membership value is calculated on the per rule basis. The input memberships and the weighted average of the output values gives the below expression

$$u = \frac{\mu_1 u_1 + \mu_2 u_2 + \cdots + \mu_n u_n}{\mu_1 + \mu_2 + \cdots + \mu_2} = \frac{\sum_{n=1}^{\#\ of\ rules} \mu_n u_n}{\sum_{n=1}^{\#\ of\ rules} \mu_n} \tag{3.19}$$

Where μ_n is, the input of the membership and u_n is the center values of the output for rule n.

There is a lot of type of fuzzification and defuzzification strategies. Thus, constraints on the Fuzzy Logic Controller is given a linear approximation of typical Fuzzy Logic Controller applications. Hence, the fuzzification process, defuzzification process, and the knowledge base can be constrained as follows:

1- The fuzzification process used the triangular shape for membership functions. The triangular membership function has only one value at a specific point where the membership is one, and this point of the membership is decreased linearly to zero on each side.

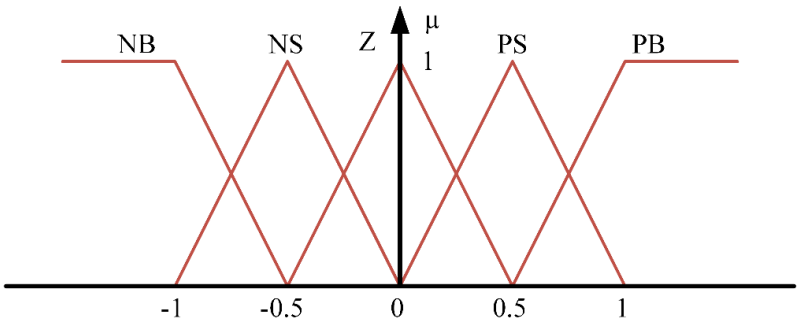


Figure 3.8. Membership functions for FLC

2- A fuzzy set width is extended to the maximum value of every adjacent fuzzy set and vice versa, as shown in Figure 3.9. The summation is one of the membership values over the region between two adjacent sets. Therefore, this means the summation of all membership function value is one over the universe of discourse at any moment for control system variables.

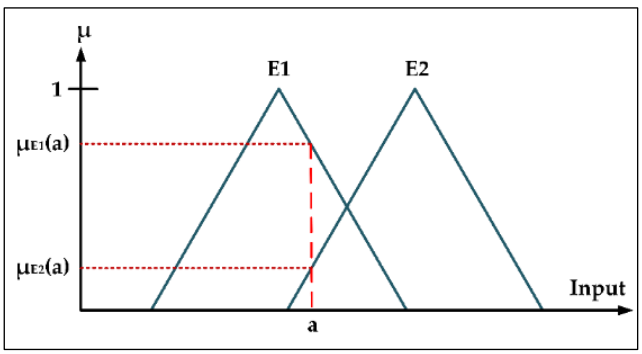


Figure 3.9. Triangular memberships

The defuzzification processing that is used is the center of gravity. The center of gravity is used to obtain the weighted average of all applicable output values. Therefore, these components are linear.

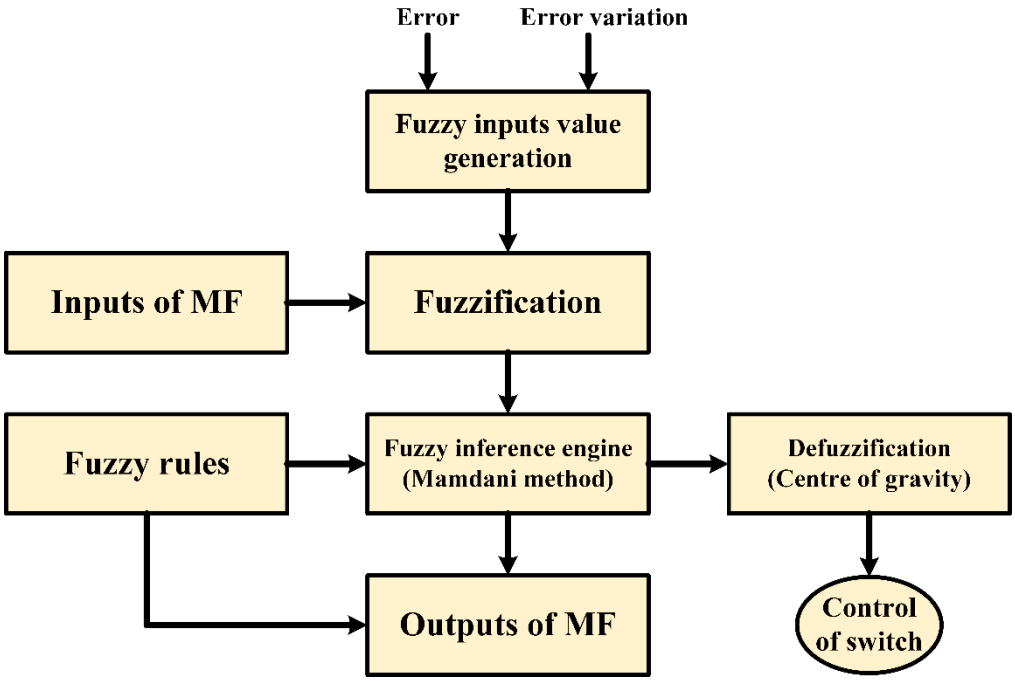


Figure 3.10. Flowchart of proposed FLC

However, the structure of the fuzzy control rules is heuristic in nature and is based on the following criteria [86]:

1. The change of duty cycle must be significant to bring the output to the setpoint quickly if the output voltage of the converter is far from the voltage reference.
2. A small change of duty cycle is required if the output of the converter is approaching the set point.
3. The duty cycle must be fixed to prevent overshoot if the output voltage of the converter is near the setpoint and is approaching it rapidly.
4. The duty cycle must be changed just a little bit to prevent the output from moving away if the setpoint is reached and the output is still evolving.
5. The duty cycle does not need to change if the setpoint is reached, and the output is steady.
6. The sign of the change of duty cycle must be negative, and vice versa, if the output is above the set point.

According to the above criteria, the rules can be written, as shown in Table 1. The entries of the table are the normalized singleton values of the variations of the duty cycle.

Table 3.1. Fuzzy rule matrix

e / e'	NB	NS	Z	PS	PB
NB	NB	NB	NB	NS	Z
NS	NB	NB	NS	Z	PS
Z	NB	NS	Z	PS	PS
PS	NS	Z	PS	PB	PB
PB	Z	PS	PB	PB	PB

The decision making logic results have collected all value of firing wight f and degree of duty cycle variation C_i that gotten fuzzy product inclusion

$$y_i = prod[U(e), U(e')] \times C_i = f_i \times C_i \tag{3.20}$$

y_i is a variation of duty cycle concluded by the i-th rule. y_i is a linguistic value that is needed to translate into the output control function of fuzzy logic by defuzzification processing. The described equation of fuzzification processing by using the center of gravity can be written as follow:

$$\delta d_i = \frac{\sum_{i=1}^{4} y_i}{\sum_{i=1}^{4} f_i} \tag{3.21}$$

The output of the controller is the duty cycle, and it can be defined as:

$$d_i = d_{i-1} + \beta \delta d_i \tag{3.22}$$

Where δd_i is the deduced change of duty cycle by the fuzzy controller at the i-th sampling time and β is the gain factor of the fuzzy controller, which can change the sufficient gain of the controller by varying the β[85, 87]. If the magnitude of the deduced change of duty cycle is 1, the duty cycle will be changed in full strength, which is limited by β.

3.3. Proportional-Integral (PI) Controller

The Proportional-integral (PI) CONTROLLER is feedback loop control and has many applications in the industrial region. The PI control reduces the error between the desired value and measure value by calculating and then the control output correct and adjust the system processing according to the requirements[88]. The calculation processing of PI control includes the two separate values, Proportional, and Integral values. Then the described transfer function of the PI controller [89] is written as:

$$u(t) = K_p + \frac{K_i}{s} \tag{3.23}$$

Where K_p and K_i are proportional and integral gain values, respectively, the proportional constant makes the dynamic response more stable by responding to changes that occur in the measured error value. The Ki makes the steady-state error magnitude to zero [90, 91]. The settling time and peak overshoot must take into account when choosing the values K_p and K_i. Figure 3.11. shows a block diagram of the PI control structure.

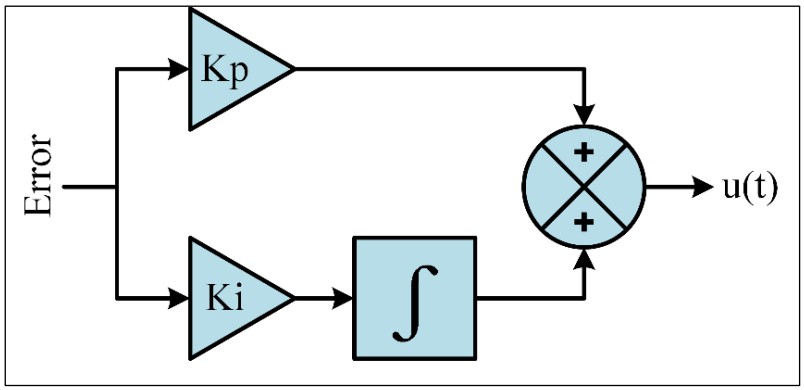


Figure 3.11. PI control scheme

The output of the proportional part results from multiply the constant value (K_p) by the error value.

$$P_{out} = K_p \cdot e(t) \tag{3.24}$$

Where P_{out} is the output of the proportional term.

The big value of proportional gain leads to a large in the output for calculated change in the error value. While the small gain produces a little response in output to big error value and control sensitivity becomes low.

The integral part results from the summation of the instantaneous error over time. It gives the calculated offset that needs to correct previously. The calculated error will multiply by a constant value (K_i) and then to the output of the controller.

$$I_{out} = K_i \cdot \int e(t) \tag{3.25}$$

Where I_{out} is the output of the integral term.

The integral part, when summed with the proportional part, makes the system processing faster to bring the system to the desired reference. Also integral part has an advantage that is canceled the residual steady-state error, which is resulted from the proportional gain.

3.3.1. PI tuning

The wrong choice of PI controller parameters leads to make the system unstable that means the output of the system goes far away from the desired reference with or without oscillations, as shown in Table 3.2.thus, the PI controller needed to tune its parameters. The tune processing means the PI control loop is the adjustment of the control parameters.

Table 3.2. Increasing of PI parameters effects.

Parameter	Overshoot	Rise Time	Settling Time	Steady-state error
K_p	Increase	Decrease	Small Change	Decrease
K_i	Increase	Decrease	Increase	Cancel

There are many tuning methods are discussed by researchers. One of these methods is the Ziegler- Nichols that is used for tuning the parameters of the PID controller [92, 93]. This mothed is commonly used in some industrial applications with some improvement in its rules. Ziegler- Nichols rules (see Table 3.3.) are used to improve the closed-loop system with

good response against load disturbances. These rules are the most popular berceuse; they are simple and easy to understand [93].

Table 3.3. Ziegler-Nichols tuning rules.

Parameter	Kp	Ki	Kd
P	$0.5\ K_u$	———	———
PI	$0.45\ K_u$	$0.54\frac{K_u}{T_u}$	———
PID	$0.6\ K_u$	$1.2\frac{K_u}{T_u}$	$0.6\frac{K_u T_u}{8}$

Ziegler-Nichols tuning rules are intended to achieve a (¼) decay ratio in closed-loop response, as shown in Figure 3.12.

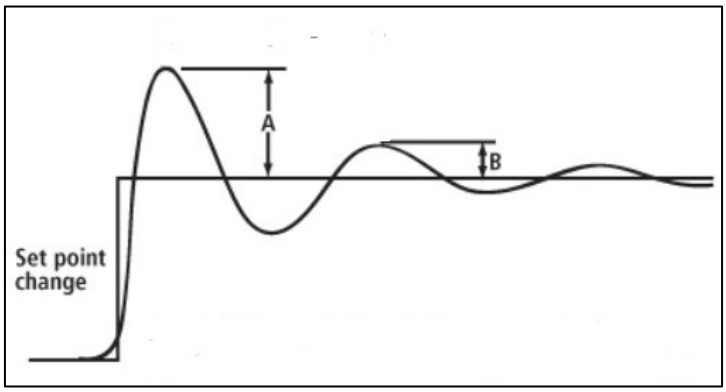


Figure 3.12. Response decay rate (B=¼ A)

By applying these rules on equation (2.3) and using the PID tune tool in Matlab/Simulink , the PI parameters are Ki=72 and Kp=1. The step response of the system is shown in figure 3.13.

3.3.2. PI control limitations

PID or PI controller is used early in industrial applications because of its advantages such as Economical cost, robust and parameter tuning is easy and simple [93]. In other, the PI controller has some disadvantages that make it is not favored selection in some cases that can summarize as follow [56, 57]:

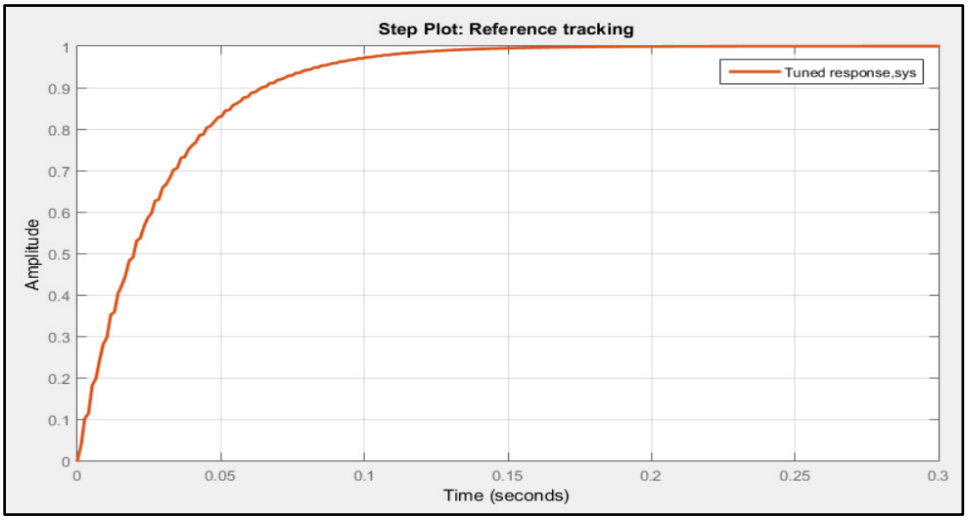


Figure 3.13. The step response of the system with selected PI parameters

The performance of PID control types is not very well in the non-linear system because it is linear control. Thus, it has stability limitations around the operating points and does not apply to these systems.

Besides, the PI is not robust against variations of the parameter with time. The parameter variations can be affected by heating or noise, which are increasing deployment of microgrids and smart grids, constant power loads are increasing gradually [18-24].

Some PID controller has been improved its performance by using other mothed such as FLC or gain scheduling [94].

3.4. Field Programmable Gate Arrays (FPGAs)

In 1985, the first concept of Field Programmable Gate Arrays (FPGA) introduced by the Xilinx company. FPGA aimed to unite time to market of programmable logic devices (PLD) and user control with cost benefits intensity of gate array. FPGAs are one class of programmable logic devices (PLDs). The FPGA is consist of flip flops and logic block, which are formed as a two-dimensional array [95]. The FPGA differs from DSP or other microprocessors due to its interconnections that have electrically programmable among logic blocks while in other custom microprocessors, form metal technology is used. In other words, the other processers have the permanent hardware configuration that means the transistors, interface structures, registers, and all of the connections are permanent, while the

FPGA is not the fixed hardware configuration. FPGA is configurable, which means the hardware configuration of FPGA is not fixed. The end-user can be defined as the FPGA hardware configuration. Thus, FPGAs allow the users to achieve digital logic operations of varying complexities. They can be more effectively used for control processing. The user can be delivered digital logic functions of varying by configuring the FPGA. FPGAs can be very effectively used for control desire in processes requiring a faster loop cycle [96, 97].

Table 3.4. Processer vs. FPGA

Criteria	Processor	FPGA
Hardware structure	Fixed	Flexible
Cost	Low	High
power	Not efficient	Efficient
Execution	Sequential	Concurrent
Programming	Assembly language	HDL
Development time	Short	Long

3.4.1. FPGA architectures

Today, there two FPGA families are the most commonly used around the world, which are Xilinx and Altera FPGAs. Each FPGA family has its architecture, but, in general, has the fundamental blocks, as shown in Figure 3.14. The underlying FPGA architecture consists of Logic gates also blocks an adaptive logic module named Altera vonder, input/ output blocks, and programmable interconnect that is configurable. Besides, the clock circuity to drive the clock signal for every block. Another logic resource may be available like an Arithmetic logic unit (ALU), decoders, and memory. Herein the Altera's FPGA cyclone family is introduced[95, 96].

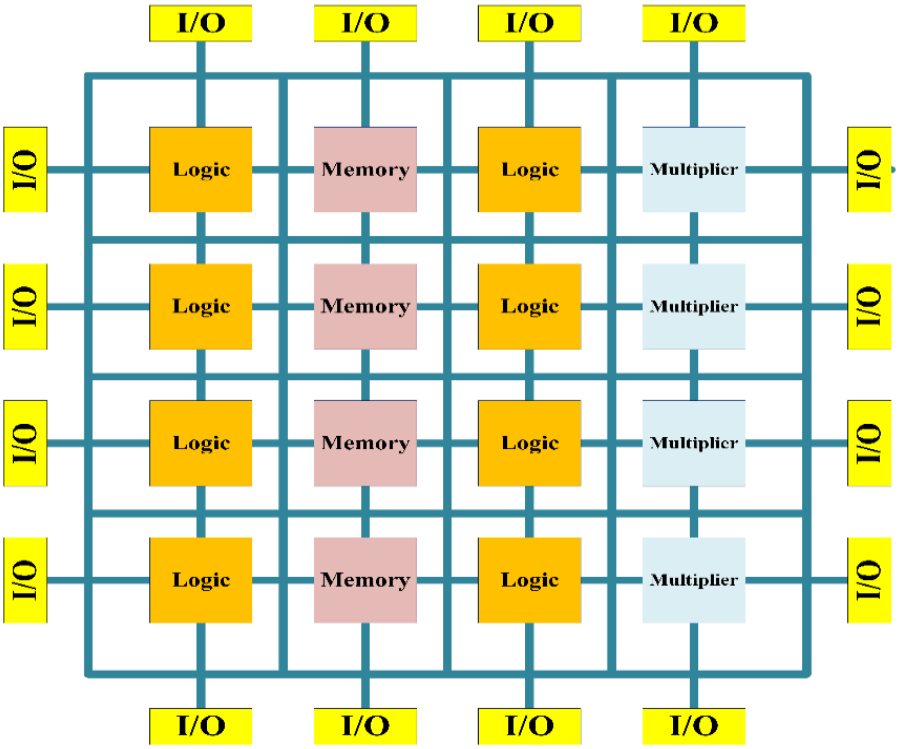


Figure 3.14. FPGA architectures

Adaptive logic module

The Altera's configurable logic blocks (CLB) is named adaptive logic module (ALM). Each ALM consists of four registers within ports such as clock Data, Synchronous, and asynchronous clear and Synchronous load, as shown in Figure 3.15. Each ALM can achieve all required functions with six input function and another up to seven input functions. The ALM have four-mode operations as below:

1. Normal Mode: combinational functions implementation and are doing.
2. Extended LUT Mode: the implementation of a specific set of seven input functions is done.
3. Arithmetic Mode: adders, accumulators, counters, functions, wide parity, and comparators are implemented .and also clock enable, add and subtract control, synchronous up and down control, synchronous clear, counter enable, and synchronous load.
4. Shared Arithmetic: the improvement of the adder tree is achieved by reducing the summation stages.

The selection of operating mode is made automatically by using The Quartus II Compiler.

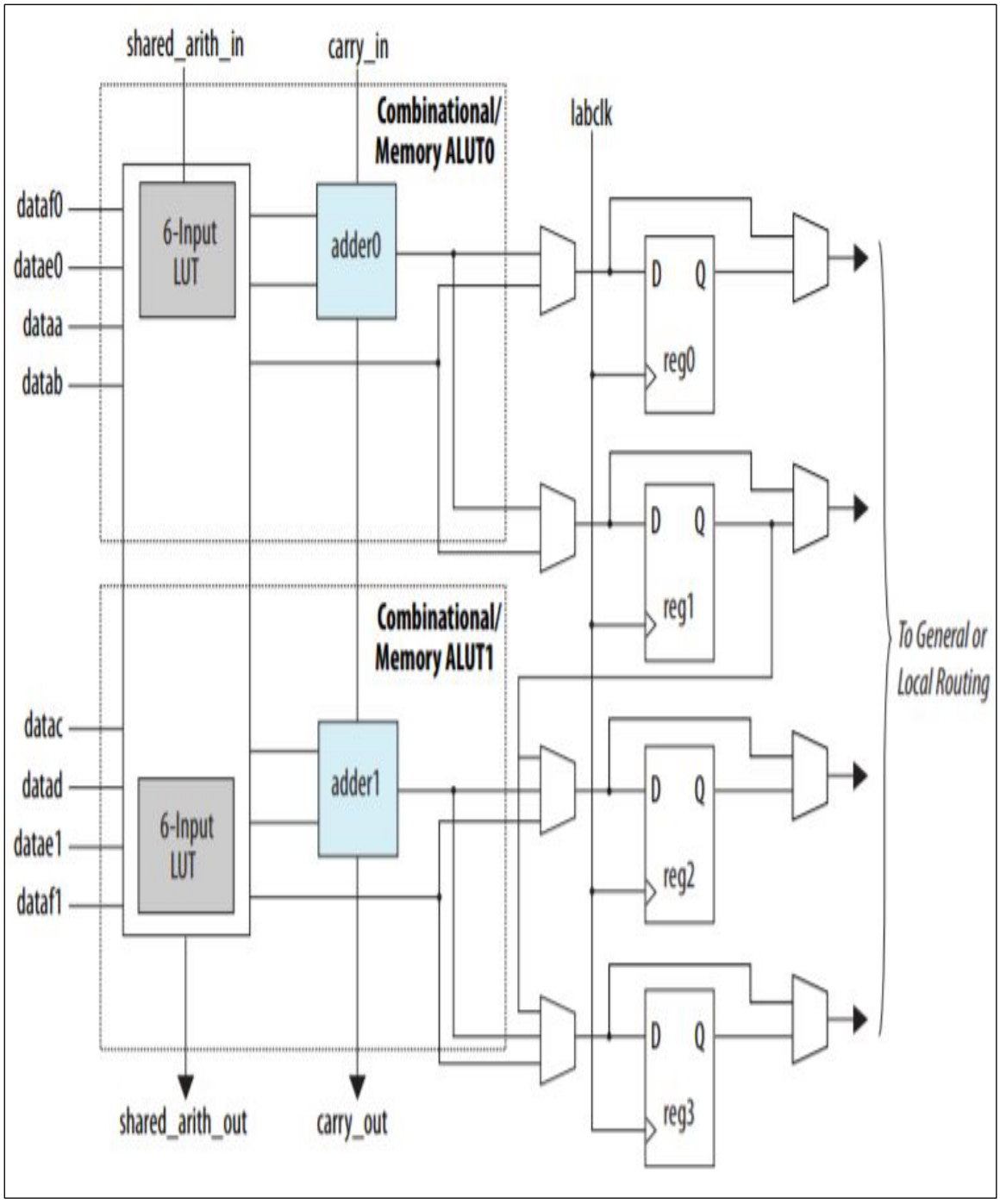


Figure 3.15. Adaptive logic module (ALM) © Altera

Input/output blocks

The connection type of input/output blocks among their buffers and register depends on the family and version of the FPGA. For in Figure 3.16., the interconnected of the input/output

element of The Altera Cyclone IV. The connection is bidirectional among the five registers and buffer. It allows registering the inputs and outputs.

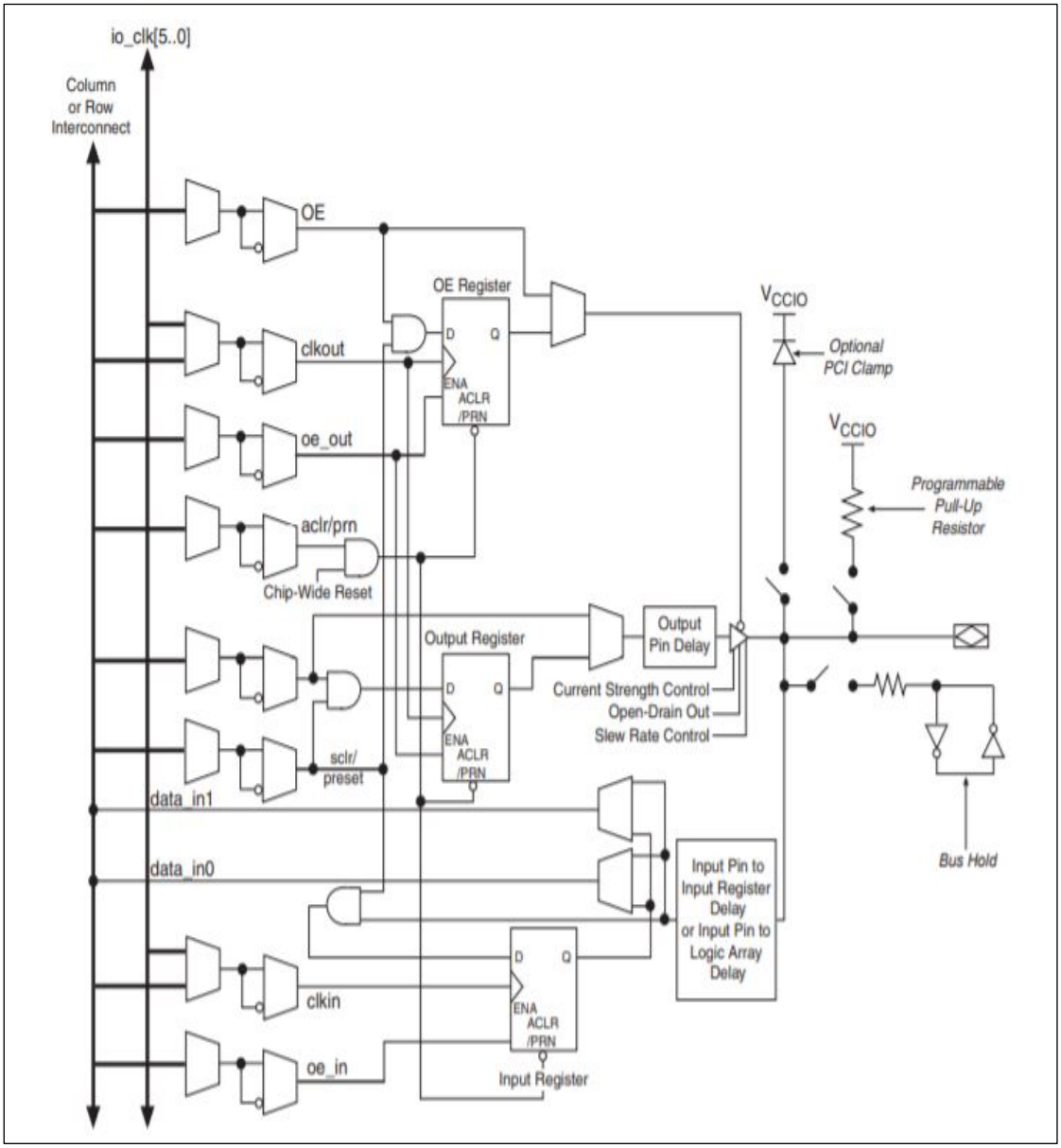


Figure 3.16. Interconnected of input/output element © Altera

Programmable interconnected

The programmable interconnected for an FPGA is a similar Application Specific Integrated Circuit (ASIC). It is a long (see Figure 3.17), but it provides to connect faster among the ALMs (CLB) that are far physically. Also, it can be used as buses on the chip. There is also the short line that is connected between individual CLBs. The programmable switch on the

chip that is used to connect interconnected lines with another interconnected line, CLBs and switch matrix. There are global clock lines that are connected to the connecting element in FPGA with the FPGA clock. They have distributed the clocks through the FPGA architecture[98].

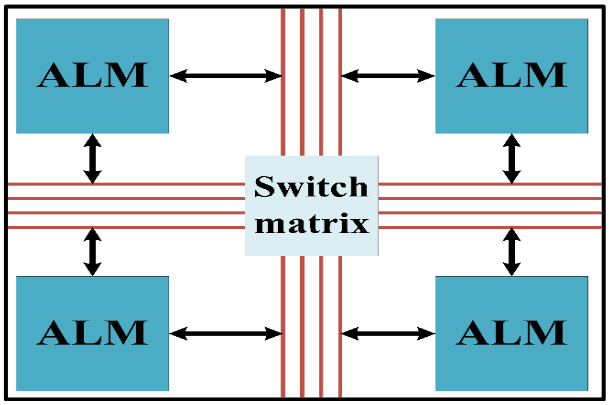


Figure 3.17. Programmable interconnected

Clock circuity

The clock circuity is individual input/ output blocks with high drive clock buffers. Also called a clock driver, and it distributes around FPGA structure. They have connected the globally interconnected lines with clock input ports. They must design as synchronous design to provide low skew time and fast propagation[98].

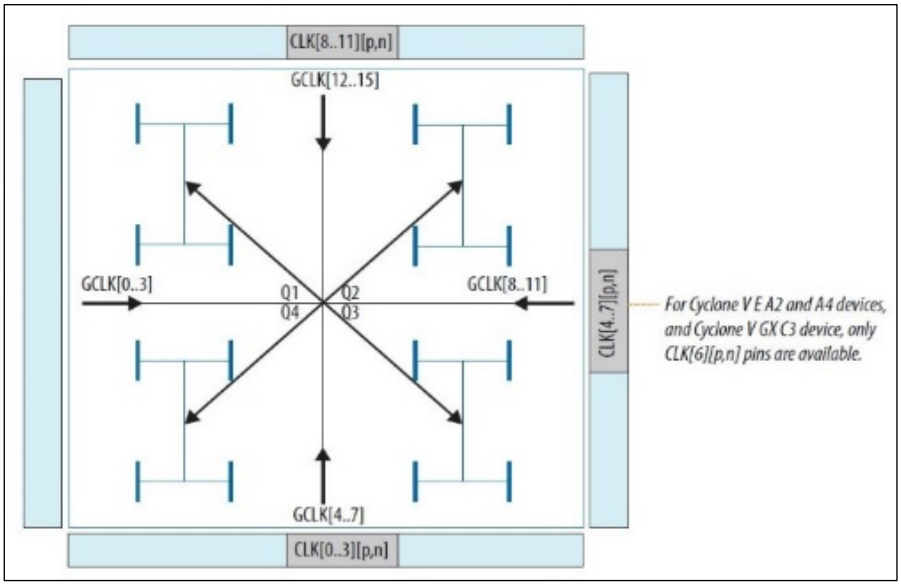


Figure 3.18. Clock circuity

3.4.2. Quartus II

The Altera software tool is called Quartus II. Quartus II capable of designing the digital logic circuit. The Quartus II tool is an automated system for the end-to-end design of digital devices based on FPGAs from Altera [99]. It provides the user with ample opportunities for entering project descriptions, logical synthesis, compiling a project, FPGA programming, functional and temporal modeling, brief analysis and analysis of project power consumption, and implementation of intersystem debugging.

The Quartus II tool contains the SOPC (System on programmable chip) Builder tool for designing processor systems implemented on a chip. Using this tool, you can easily create configurable processor cores, deploy various controllers on a chip, as well as a significant part of peripheral equipment. However, the Quartus II tool flow is shown in Figure 3.19. The Quartus II tool makes the project design more comfortable for the designer to do the desired logic [96].

3.4.3. Hardware description language

A hardware description language (HDL) is a specific programming language uses to characterize or describe the architecture, behavior, simulation of the digital circuit. There many types of HDLs, but the most commonly used language are Verilog and VHDL. They can use for describing a digital circuit that has a parallel operation model. In Other Conventional programming languages, their program is based on a sequential operation model. This means they are unable to be guaranteed description and simulation of the operation of the digital circuit. In this thesis, the used HDL is Verilog [96, 100].

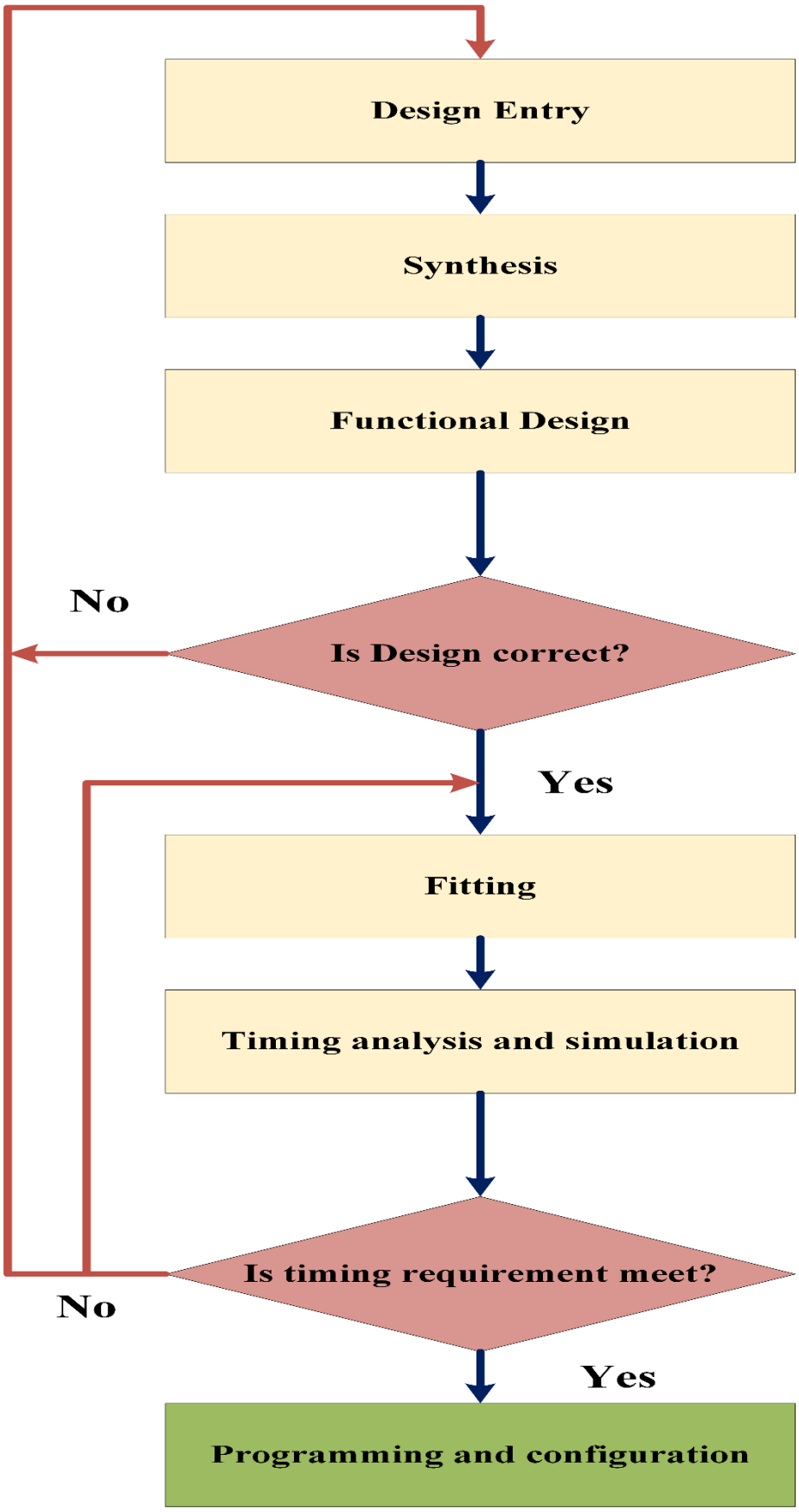


Figure 3.19. FPGA CAD design

3.4.4. FPGAs design advantages

FPGAs have many advantages compare to another ASIC or DSP in terms of design, cost development, chance to speed products to market, reducing area, and parallel processing [101, 102].

1. FPGA introduces a more straightforward way to achieve any design. It is easy to use a software development tool to fit, simulate, and optimize the design.
2. FPGA offers the lowest development cost because it is a programmable device; therefore, the design changing is easier.
3. FPGA has a large number of gates per area with a tiny size factor package. It has thus provided the ideal solution for users.
4. One of the best benefits of using FPGA for project design is parallel processing. Figure 3.20. shows the basic concept of parallel processing. The control core can switch the inputs and output data rotationally. Then a new input data can apply to inputs of DSP cores each clock cycle. This means the DSP blocks can operate in a parallel on one sequential stream of incoming data.

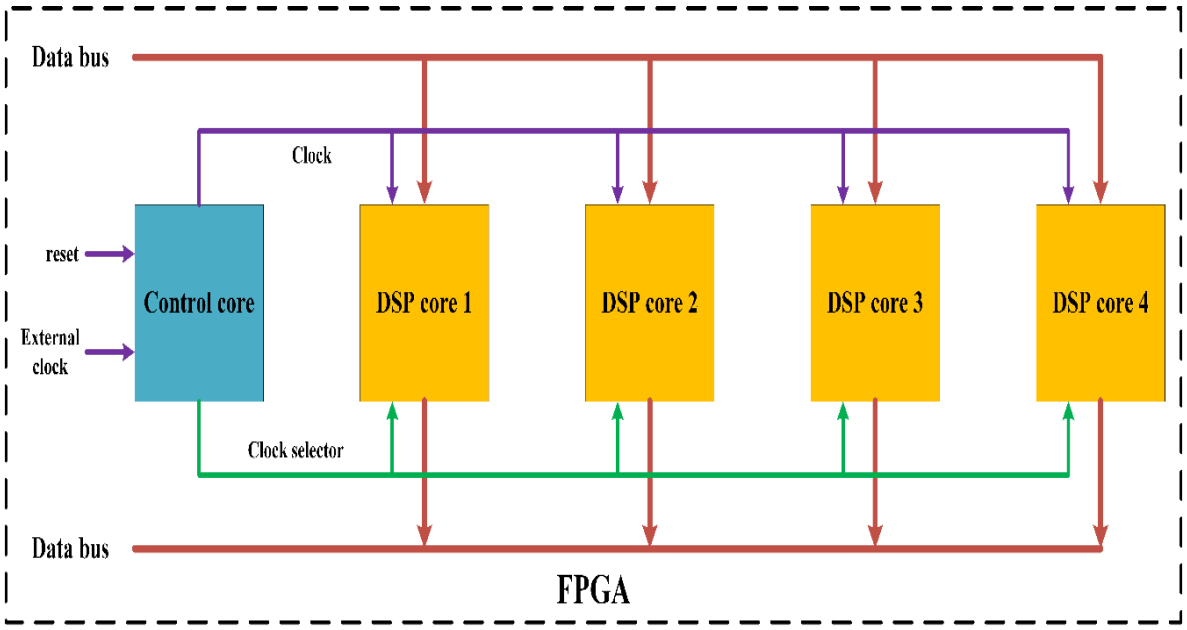


Figure 3.20. Parallel processing

3.4.5. FPGA based fuzzy logic controller for electric power system: an overview

FLC is used widespread for real-time applications. Hardware-based solutions and software-based solutions are used for FLC applications. Hardware-based solutions are achieved at a high speed of inference, but they do not have flexibility. In contrast, the main properties of software-based solutions are flexible, but they have limitation speeds [30]. The FPGA provides solutions to overcome flexibility and speed limitations in both the hardware-based solutions and software-based, respectively [26, 30].

At present, like processor-based control systems, FPGAs have been used to implement all types of industrial control systems, including analog process control, discrete logic, and batch or state machine-based control systems. The field-programmable gate arrays (FPGAs) have widespread applications in the power system because they have faster processing[103]. Also, the internal connections of FPGAs can change as required functions due to the interconnections between logic blocks of these devices is electrically programmable. For these reasons, the FPGAs differ from other integrated circuit FPGA-based control systems that differ from processor-based systems in significant ways [26].

The modeling and co-simulation of fuzzy logic control by using FPGA-in-the loop for DC-DC boost converter loaded constant power load (CPL) introduced in [89]. It discussed the regulated voltage of the boost converter, which is feeding constant power load.

The 3-level space vector modulation NPC inverter for a permanent magnet synchronous machine (PMSM) is presented in [104]. The co-simulation environment implemented the proposed control by using an FPGA-in the- loop. The speed control is performed by the improvement of adaptive of the fuzzy logic control for DC motor based FPGA based on hardware implementation in [105]. The optimization of fuzzy logic used as MPPT of a stand-alone photovoltaic system using FPGA presented in [106].

Authors in [103] are presented Sugeno type fuzzy logic controller design and implementation using VHDL. They examined the fuzzy system with different membership functions for the second and third-order systems. The FPGA in the loop and real-time tests are done by using FPGA (see Figure 3.21.).

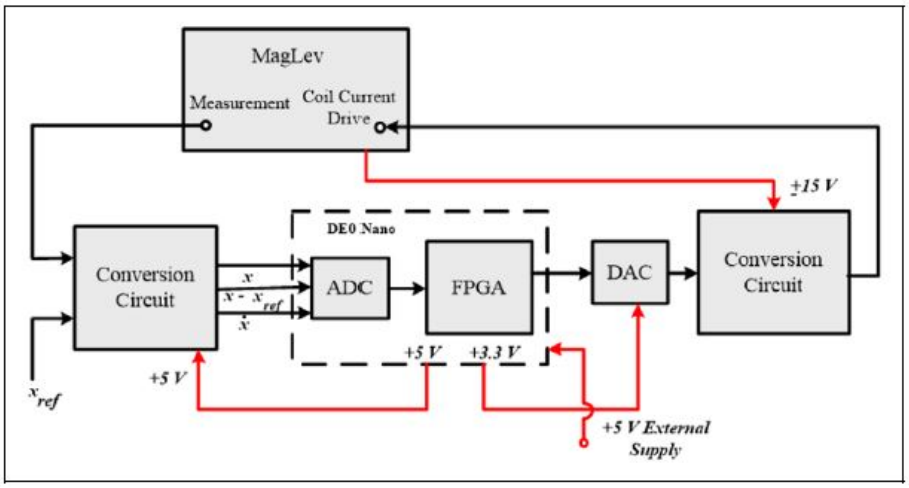


Figure 3.21. Block diagram for real-time implementation

Authors in [107] used the concept of average weight to save the fuzzy system lookup table small. The fuzzy system is implemented by using FPGA, as shown in Figure 3.22. Three or four bits represent each input to address the lookup table. Also, the same mothed is applied in [108] to control the variable speed generator.

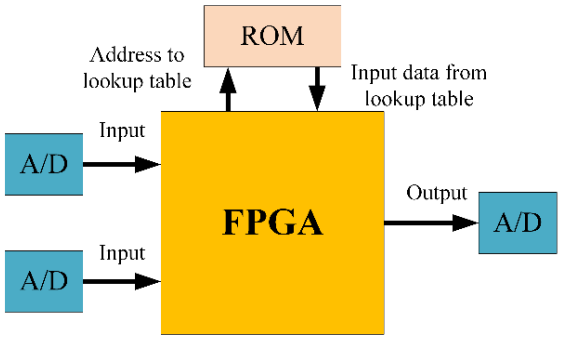


Figure 3.22. Fuzzy logic control with FPGA

Authors in [109] are used the fuzzy logic DTC to control the matrix inverter that is fed the induction motor. Also, the Authors in [110] are used the fuzzy logic controller to improve the torque ripple in the low speed of permanent magnet synchronous motor (PMSM). The FLC is used rather than hysterics controller in the conventional strategy of the direct torque control (DTC) for PMSM. The Verilog is used for describing a DTC strategy of PMSM.

Authors in [106] are introduced the optimization and implementation of THE fuzzy system that used as a maximum power point tracker in the standalone photovoltaic energy system.

The genetic algorithm is used for optimizing the membership functions and fuzzy rules. The FLC is applied to a system using Xilinx FPGA and VHDL language for writing codes (see Figure 3.23).

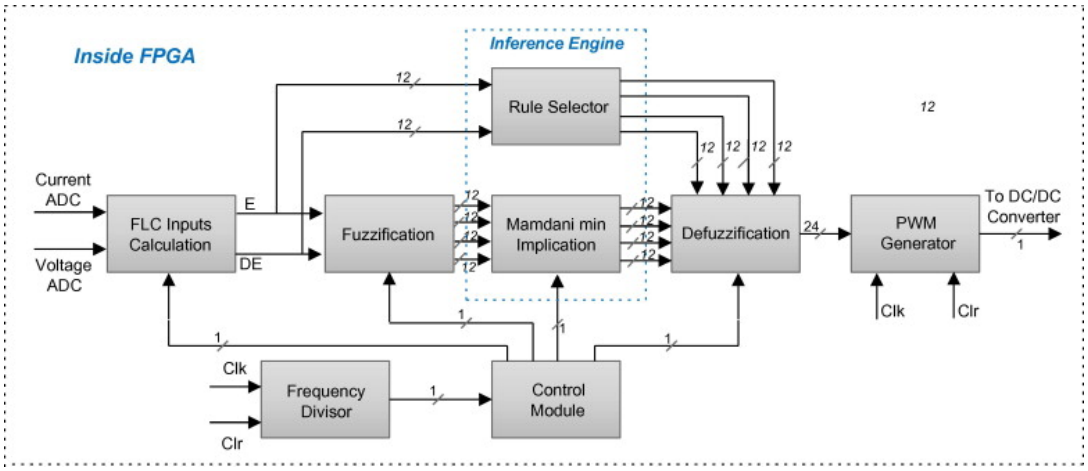


Figure 3.23. FPGA implemented MPPT

3.4.6. FPGA in the loop simulation (co-simulation mothed)

Researchers are using simulation tools extensively that are provided the perfect tools to simulate the control algorithms and mathematical modeling for any system without damage risks [88, 111]. Simulation is achieved by electronic design automation (EDA). The EDA simulator link introduces a verification interface between the HDL simulator (and FPGA board) and Simulink tools (Matlab). By using co-simulation, the verification operation between the Verilog HDL design and the Matlab/Simulink model is performed[112]. Using the EDA simulator link is allowed researchers to implement the hardware verification on the FPGA board by using FPGA in the loop (FIL) simulation. The Matlab/Simulink environment provides the toolbox and functions for HDL and FIL.

The FIL has advantages of hardware and software and their approach. The FIL has used the capabilities of Matlab/Simulink during co-simulation processing. The control algorithm runs in real-time when it is loaded to the FPGA board by using FIL. During the FIL processing, the components of the system, such as electronic power elements, sensors, and other electrical elements are simulated on Matlab/Simulink [88, 89, 113].

In FPGA-in-the loop, at each time step, the plant model is simulated in the Matlab/SimPower Systems, and then the Simulink output signals are exported to the FPGA. When the FPGA receives signals from the Simulink, it executes the implemented program for one sample interval. The FPGA returns the control signals computed during this step to Simulink. At this point, one sample cycle of the FIL is performed. In this case, a Joint Test Action Group (JTAG) interface between the Simulink and the FPGA board links both [89].

In Matlab/Simulink environment, the Verilog code of the control system can be generated by an HDL Workflow Advisor, and then this code is synthesized and fitted automatically with the Altera Quartus II software for Altera FPGA boards. In this stage of the procedure, the report files are checked for any errors or warnings. After debugging, the FIL block is instilled, and all the control system blocks are removed. Then, the Verilog code is implemented on FPGA. Figure 3.24. shows the code conversion and verification process in the MATLAB /Simulink HDL Coder.

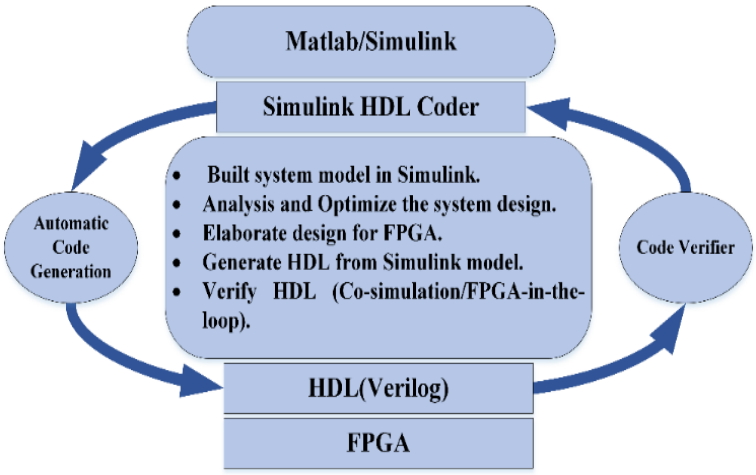


Figure 3.24. Flowchart of FIL processing

To achieve this purpose, some requirements are needed; MATLAB/Simulink, Fixed-Point Designer, Hardware Description Language HDL Verifier, FPGA design software, one of the supported FPGA development boards and accessories, and for the connection using Ethernet: Gigabit Ethernet Adapter installed on host computer, gigabit Ethernet crossover cable, and for the connection using JTAG: USB Blaster I or II cable and driver for the Intel FPGA boards: Digilent® JTAG cable, and a driver for the Altera FPGA boards.

Data type conversion

The FPGA executes the Verilog HDL or Verilog codes by using fixed-point data. The Verilog HDL supports different types of data: integer, real, and Boolean and std_logic, but it does not support the Floating-Point data type. For this reason, the implementation of Verilog HDL should be done in the fixed-point algorithm.

Singed 20-bit fixed-point data of outputs of rule base to map [-1, 1] shown in Figure 3.25. The first bit is a sign (1 for negative and 0 for positive); however, the maximum and minimum expected values for the variables can be calculated as below:

$$\begin{aligned} &\text{Maximum value} = 2^{N-1} - 1 \ (N = 20, \text{ it equals to } 1048574) \\ &\text{Minimum value} = -2^{N-1} \ (N = 20, \text{ it equals to } -1048575) \end{aligned} \tag{3.26}$$

	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	6	7	8	9	10
-10	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-0.9000	-0.8000	-0.7000	-0.6000	-0.5000	-0.4000	-0.3000	-0.2000	-0.1000	0
-9	-1	-1	-1	-1	-1	-1	-0.9854	-0.9683	-0.9482	-0.9240	-0.9000	-0.8000	-0.7000	-0.6000	-0.5000	-0.4000	-0.3000	-0.2000	-0.1000	0	0.1000
-8	-1	-1	-1	-1	-1	-1	-0.9708	-0.9367	-0.8964	-0.8480	-0.8000	-0.7000	-0.6000	-0.5000	-0.4000	-0.3000	-0.2000	-0.1000	0	0.1000	0.2000
-7	-1	-1	-1	-1	-1	-1	-0.9562	-0.9050	-0.8445	-0.7720	-0.7000	-0.6000	-0.5000	-0.4000	-0.3000	-0.2000	-0.1000	0	0.1000	0.2000	0.3000
-6	-1	-1	-1	-1	-1	-1	-0.9415	-0.8733	-0.7927	-0.6960	-0.6000	-0.5000	-0.4000	-0.3000	-0.2000	-0.1000	0	0.1000	0.2000	0.3000	0.4000
-5	-1	-1	-1	-1	-1	-1	-0.9269	-0.8417	-0.7409	-0.6200	-0.5000	-0.4000	-0.3000	-0.2000	-0.1000	0	0.1000	0.2000	0.3000	0.4000	0.5000
-4	-1	-0.9817	-0.9664	-0.9533	-0.9420	-0.9321	-0.8538	-0.7625	-0.6545	-0.5250	-0.4000	-0.3000	-0.2000	-0.1000	0	0.1000	0.2000	0.3000	0.4000	0.5000	0.6000
-3	-1	-0.9635	-0.9327	-0.9066	-0.8840	-0.8643	-0.7808	-0.6833	-0.5682	-0.4300	-0.3000	-0.2000	-0.1000	0	0.1000	0.2000	0.3000	0.4000	0.5000	0.6000	0.7000
-2	-1	-0.9452	-0.8991	-0.8598	-0.8260	-0.7964	-0.7077	-0.6042	-0.4818	-0.3350	-0.2000	-0.1000	0	0.1000	0.2000	0.3000	0.4000	0.5000	0.6000	0.7000	0.8000
-1	-1	-0.9269	-0.8655	-0.8131	-0.7679	-0.7286	-0.6346	-0.5250	-0.3955	-0.2400	-0.1000	0	0.1000	0.2000	0.3000	0.4000	0.5000	0.6000	0.7000	0.8000	0.9000
0	-1	-0.9087	-0.8319	-0.7664	-0.7099	-0.6607	-0.5615	-0.4458	-0.3091	-0.1450	0	0.1000	0.2000	0.3000	0.4000	0.5000	0.6000	0.7000	0.8000	0.9000	1
1	-0.9000	-0.8087	-0.7319	-0.6664	-0.6099	-0.5607	-0.4615	-0.3458	-0.2091	-0.0450	0.1000	0.2000	0.3000	0.4000	0.5000	0.6000	0.6800	0.7600	0.8400	0.9200	1
2	-0.8000	-0.7087	-0.6319	-0.5664	-0.5099	-0.4607	-0.3615	-0.2458	-0.1091	0.0550	0.2000	0.3000	0.4000	0.5000	0.6000	0.7000	0.7600	0.8200	0.8800	0.9400	1
3	-0.7000	-0.6087	-0.5319	-0.4664	-0.4099	-0.3607	-0.2615	-0.1458	-0.0091	0.1550	0.3000	0.4000	0.5000	0.6000	0.7000	0.8000	0.8400	0.8800	0.9200	0.9600	1
4	-0.6000	-0.5087	-0.4319	-0.3664	-0.3099	-0.2607	-0.1615	-0.0458	0.0909	0.2550	0.4000	0.5000	0.6000	0.7000	0.8000	0.9000	0.9200	0.9400	0.9600	0.9800	1
5	-0.5000	-0.4087	-0.3319	-0.2664	-0.2099	-0.1607	-0.0615	0.0542	0.1909	0.3550	0.5000	0.6000	0.7000	0.8000	0.9000	1	1	1	1	1	1
6	-0.4000	-0.3087	-0.2319	-0.1664	-0.1099	-0.0607	0.0385	0.1542	0.2909	0.4550	0.6000	0.6800	0.7600	0.8400	0.9200	1	1	1	1	1	1
7	-0.3000	-0.2087	-0.1319	-0.0664	-0.0099	0.0393	0.1385	0.2542	0.3909	0.5550	0.7000	0.7600	0.8200	0.8800	0.9400	1	1	1	1	1	1
8	-0.2000	-0.1087	-0.0319	0.0336	0.0901	0.1393	0.2385	0.3542	0.4909	0.6550	0.8000	0.8400	0.8800	0.9200	0.9600	1	1	1	1	1	1
9	-0.1000	-0.0087	0.0681	0.1336	0.1901	0.2393	0.3385	0.4542	0.5909	0.7550	0.9000	0.9200	0.9400	0.9600	0.9800	1	1	1	1	1	1
10	0	0.0913	0.1681	0.2336	0.2901	0.3393	0.4385	0.5542	0.6909	0.8550	1	1	1	1	1	1	1	1	1	1	1

Figure 3.25. Output values of the rule base

Conversion blocks in the simulink model

The blocks in the Matlab/Simulink model can be used to Verilog HDL or VHDL codes by using HDL Workflow Advisor. The HDL Workflow Advisor generates the separate Verilog HDL code for each block in Simulink. These codes provide communications bidirectional

from and to Matlab/Simulink environment. Also, the HDL Workflow Advisor improves the design performance and help identify speed bottlenecks in Matlab/Simulink modeling.

Verification of fpga in-the-loop (FIL) co-simulation

The output block of conversion processing in the previous section is FIL block, as shown in Figure 3.26. The FIL file represents the control block in the HDL code. The verification processing implements by loading the programming file onto the FPGA via JTAG connection. The data will transmit and receive between the Simulink model and FPGA by using the Gigabit Ethernet crossover cable. This processing is co-simulation and Verification of the proposed control model in Simulink in a real-time environment.

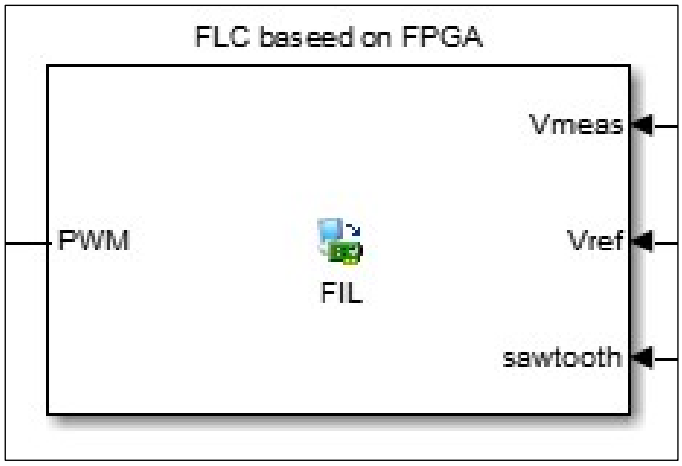


Figure 3.26. FIL file of the FLC

3.9.10. Implemented Verilog HDL codes for real-time application

The Fuzzy logic, PI controller, PWM, and clock divider codes are designed and modeled in the EDA environment using Verilog HDL. The Verilog HDL codes wrote using Notepad++ editor and Verified, synthesized, and fitted using Quartus Prime 18.1 Lite Edition. In this thesis, the designed controller is broken down into parts with each part performed a specific function such as PI, FLC, PWM, and clock divider (see index section). Thus means each design of any part easily modified and combined among components to form the desired controller. The main code has functions and called the required codes to implement the controller.

Clock divider

The internal clock of Altera DE0-Nano-SoC FPGA is 50 MHz, and then this clock is not proper in the experimental application. The clock (or called frequency)divider code is required to reduce the internal clock. The clock divider is implemented by using a counter and scaling factor (see equation (3.27.) and index-1)

$$\text{scale} = \frac{\text{internal clock frequency}}{\text{desired clock frequency}} \tag{3.27}$$

Herein, the required frequency (1 MHz) and internal clock frequency (50 MHz) need the scale is (50), which means the output signal of (1 MHz) every 50 cycles.

Fuzzy logic

The implemented design used three types of functions triangular, S, and Γ function, which is introduced (see section 3.2.2). The universe of discourse of the input member functions is divided into five fuzzy sets value (M1 to M5) with integer data type and represented 12-bit, and the output variables have five linguistic values (D1 to D5) with integer data type and represented 12-bit (see index-3). Also, the normalization inputs and output included) with integer data type and represented 16-bit.

The fuzzy rule base has 25 rules because each input has 5 membership functions. The rules are formulated by using the IF-THEN manner. The outputs are obtained as a look-up table form FIL simulation with integer data type and 11-bit for each rule. The FLC design in this thesis incorporates Mamdani's implication method of inference.

The fuzzification, defuzzification, and normalization processing require divider and multipliers. Behavioral modeling in Verilog HDL supports division and multiplication. These operations are combined to realize the implementation and synthesis stages. All the parts of the FLC are successfully designed as a top hierarchy Verilog HDL component. Figure 3.27. show the form of FLC using the Verilog HDL component.

Table 3.5. Fuzzy associative memory table

Error (e)	Change of error (Δe)					
		M^{21}	M^{22}	M^{23}	M^{24}	M^{25}
	M^{11}	C^{1}	C^{6}	C^{11}	C^{16}	C^{21}
	M^{12}	C^{2}	C^{7}	C^{12}	C^{17}	C^{22}
	M^{13}	C^{3}	C^{8}	C^{13}	C^{18}	C^{23}
	M^{14}	C^{4}	C^{9}	C^{14}	C^{19}	C^{24}
	M^{15}	C^{5}	C^{10}	C^{15}	C^{20}	C^{25}

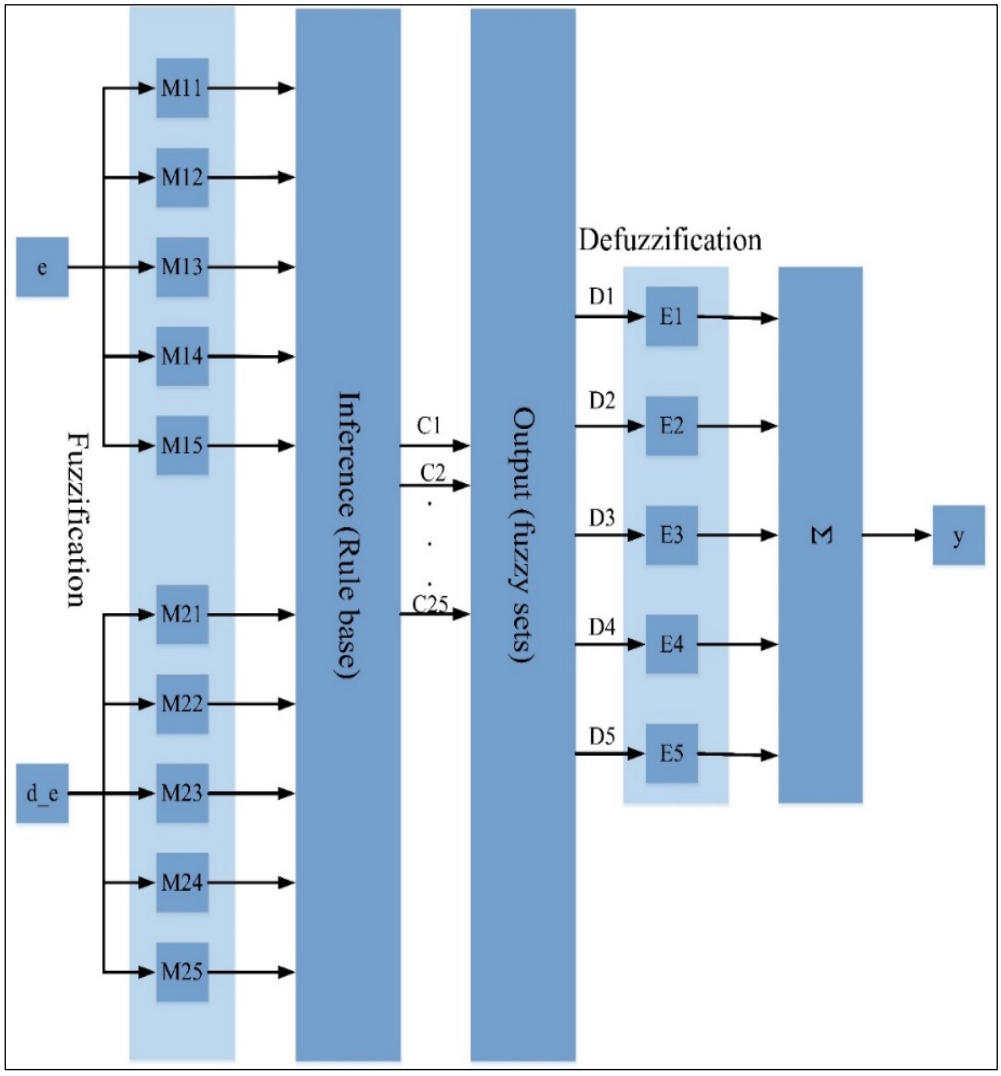


Figure 3.27. Block diagram of the operations in a fuzzy logic controller

PI controller

The Verilog HDL code of the PI controller has included the calculation of proportional and integral parts. After error calculation, the error will multiply by K_p that is proportional value with 16-bit. The integral part is calculated by accumulating the multiplication results of integral gain K_i and error (see index-2).

Pulse width modulation (PWM)

The PWM code will contain three main parts, a comparator, a sawtooth generator, and input that comes from the controller. The output of this code gives a variable duty cycle that is deepened on the output of the controller. The saw tooth frequency is 10 kHz. It is implemented hardware digitally like a simple counter (see index-4).

4. SIMULATION AND EXPERIMENTAL RESULTS

Herein, the simulation and experimental results will introduce and discuss, for the simulation results, will use the Matlab/Simulink tools and the FPGA-in-the loop. The experimental results include the implementation of the PI and FLC controllers by using the DE0-Nano-SoC Altera FPGA board and Verilog HDL language. The DC-DC buck converter selected as the source and load converter, CPL, and resistive load to build a multi converter system. The parameters of the system are depicted in Table 8.1.

4.1. Simulation Results

The system introduced in section 5.3 is considered to show the effectiveness of the designed controller. In order, this aim, the system under controller has checked different types of tests like input voltage is changed, the load step change. The system testing is done in Matlab/Simulink environment at the first step. Then to prepare the controller algorithm for the experimental test, the FPGA-in-the loop (FIL) is presented. The results of FIL are compared with the simulation results of the Matlab/Simulink toolbox.

Table 4.1. The parameters of the simulation

Parameter	Value
Source DC-DC buck converter	
V_{in}	160 V
Inductor (L_f)	1.6 mH
Capacitor (C_f)	150 µF
Resistance (R)	132 Ω
Load DC-DC buck converter	
V_{in}	120-100-80 V
Inductor (L_f)	1.6 mH
Capacitor (C_f)	150 µF
Resistance (R)	21 ohm
Constant power load	
Maximum power	300 watt

4.1.1. Simulation of FLC using Matlab/Simulink

To verify the designed FLC control in section 5.3., the multi converter system is designed and implemented using the Matlab/ Simulink environment (see Figure 4.1.). the designed circuit consists of DC voltage with 150 volts, which are feeding the first stage of the circuit. The first stage is a DC-DC buck converter with FLC as a source converter. The second is the load stage that consists of CPL, DC-DC Buck converter, and resistive load.

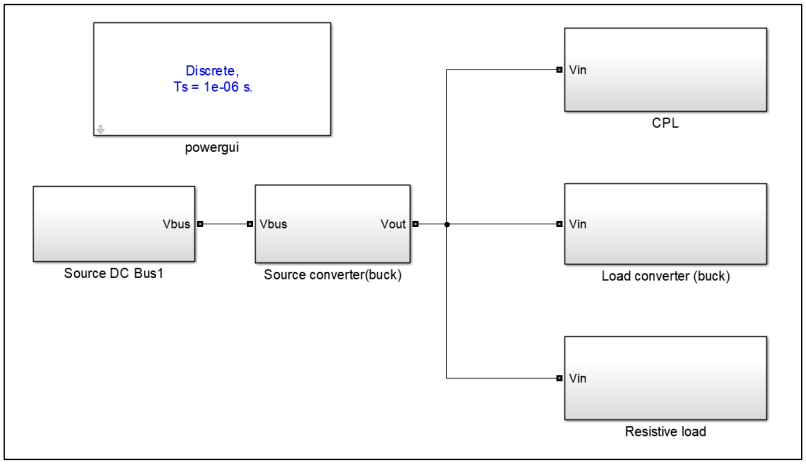


Figure 4.1. Overall system simulation

Figure 4.2. shows the DC-DC buck converter as a source converter (first stage of multi converter system) that feeds the buck converter as load converter, CPL, and resistive load as the second stage of the multi converter system.

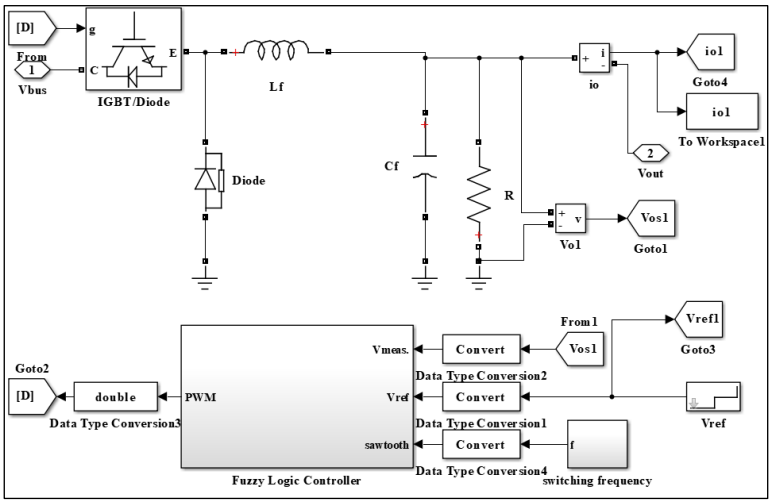


Figure 4.2. Source converter with the FLC using Matlab/Simulink environment

From Figure 3.7., the normalization parameters of error, the variation of error and output is given as Ge= 0.4, Ge'= 1×10^{-6} and Go= 0.008 respectively

Step-changing of the reference voltage

The First test is done by change the reference value of source voltage to check the FLC and to show the system behavior. Figure 4.3.a. show the good response of the controller, and the measurement value follows the reference value without overshoot occurred and matched the reference value of the voltage with small droop voltage (about 1 volt).

The voltage and current of load converter (see Figure 4.3. b and d) are also stable and constant value. the load converter did not affect by changing of feeder bus bar that is feeding by source converter.

Figure 4.3.c, show the current in resistive, which represents a linear ship between the voltage and current at a constant value of resistance value. the current is taken the form of voltage, which means the current will increase/decrease as the voltage increase/decrease.

Figure 4.3. e and f, illustrated the current and power with CPL power (150 watts), respectively. The current of CPL is decreased (2.5- 1.875- 1.5) Ampere approximately as the voltage of source converter increased (60- 80-100) volts, and it is increased as the voltage reduced to (100-80- 60) volts. Also, from Figure 4.3. the voltage will remain constant and stable after the step-up/down response.

As mention above, the designed FLC is a capable controller to regulate voltage on the main bus bar and also can guarantee the system stability under variation of the voltage reference. Another test has been done and will explain in the next section of the co-simulation and experimental results.

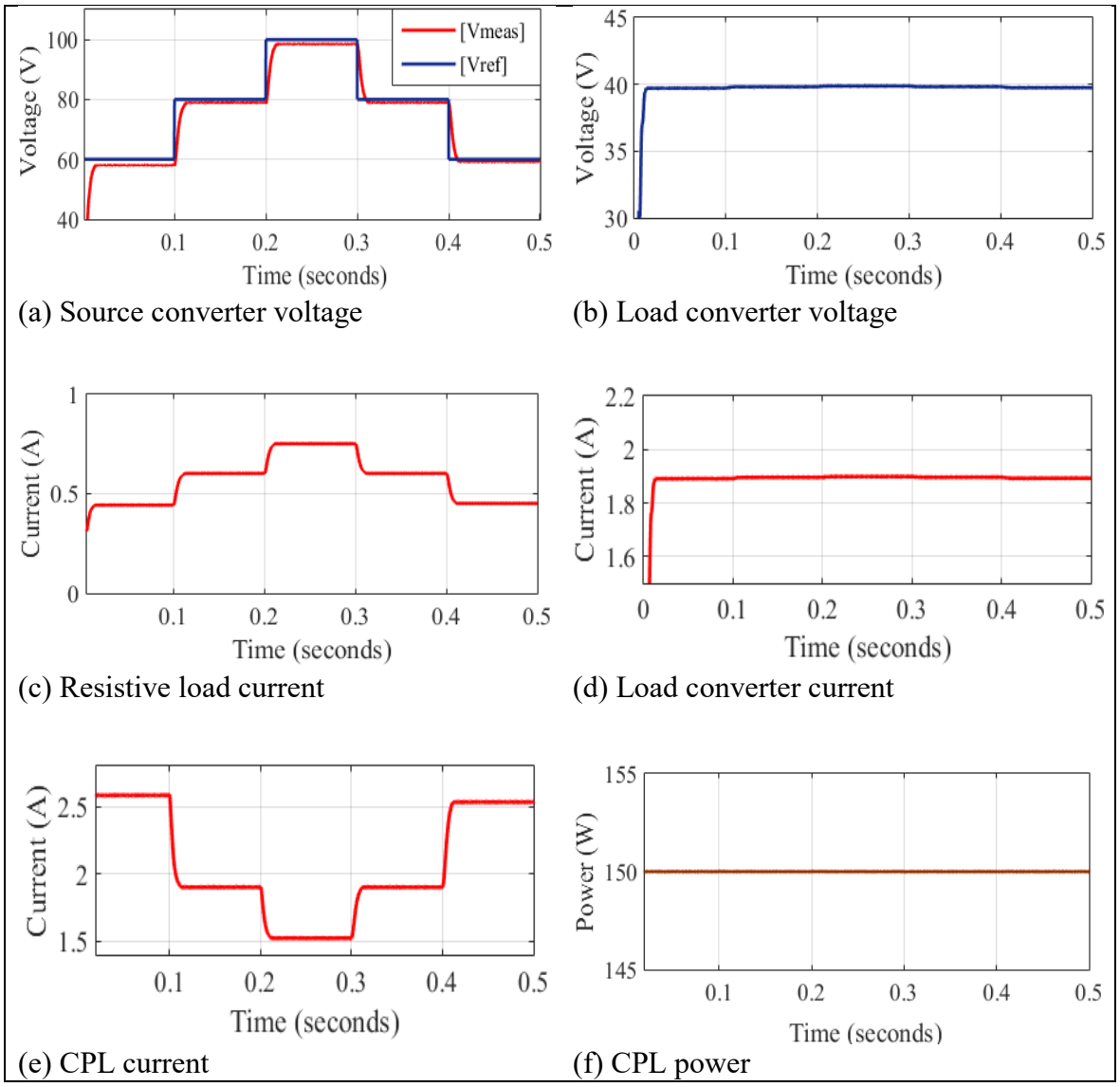


Figure 4.3. Voltage step-changing of source converter

Step power test

Herein, the step power command is designed by changing the power of the CPL from 100-150-200, as shown in Figure 4.4.f, the voltage of the source keeps constant and stable after increase/ decrease the power of CPL with small acceptable overshoot and undershoot (see Figure 4.5). Thus means the FLC controller is robust control against load variations and prevents the instability effect of CPL propagate to the system, as shown in Figure 4.4.b and d that illustrated the voltage and current of load converter. the main DC bus has constant and stable voltage due to FLC. Consequently, the voltage and current of the load converter are not affected by the step-changing of CPL power.

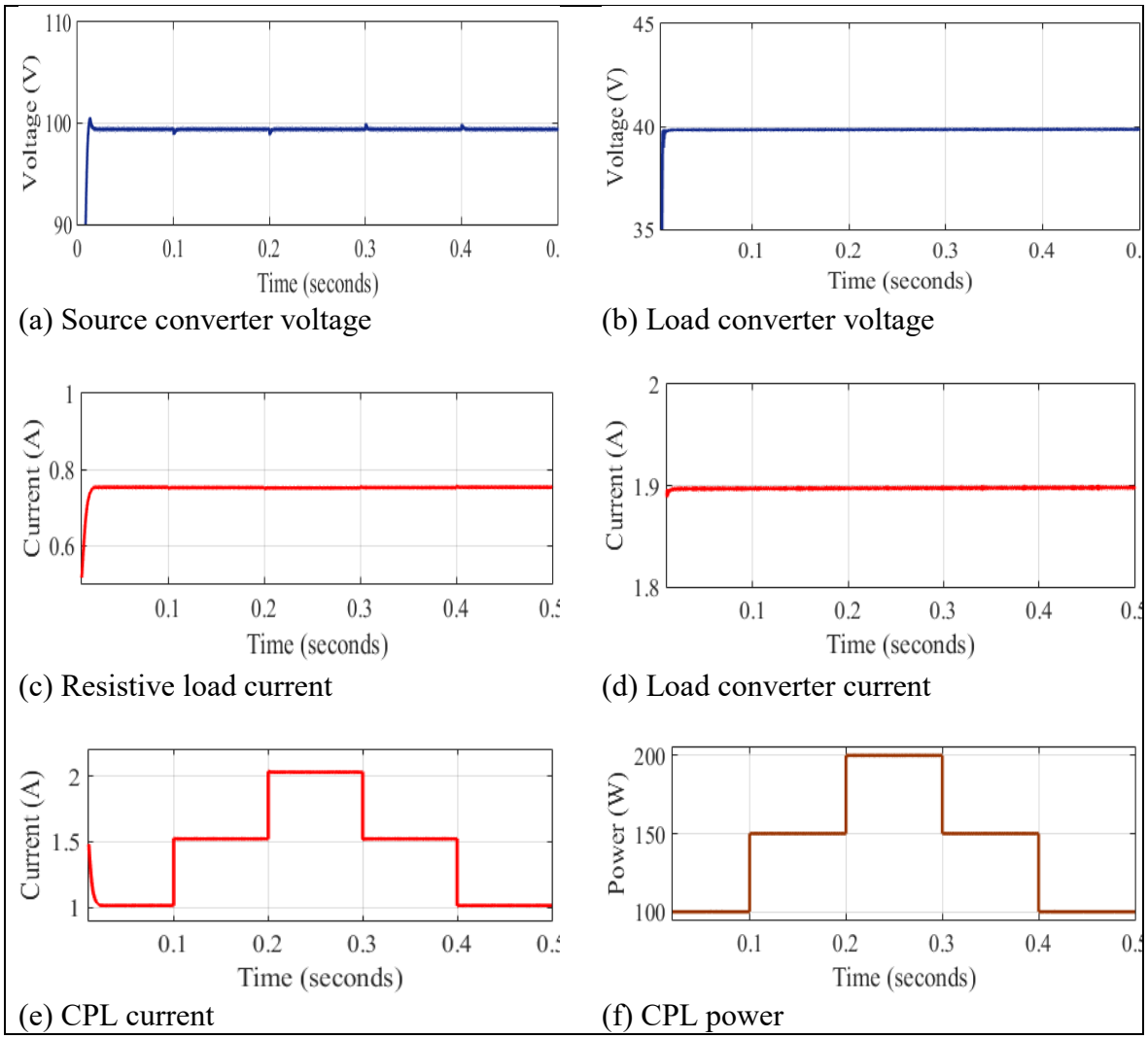


Figure 4.4. Power step-changing of CPL

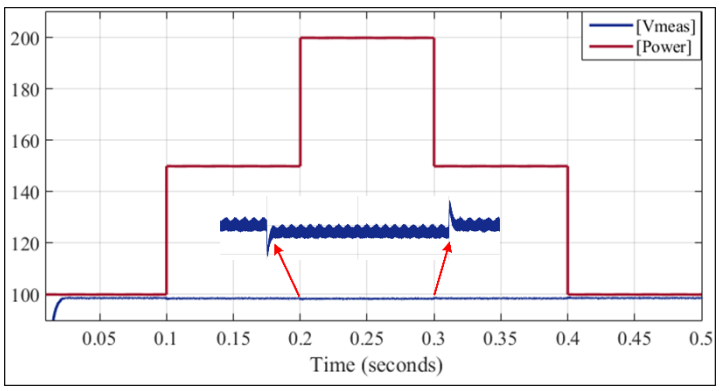
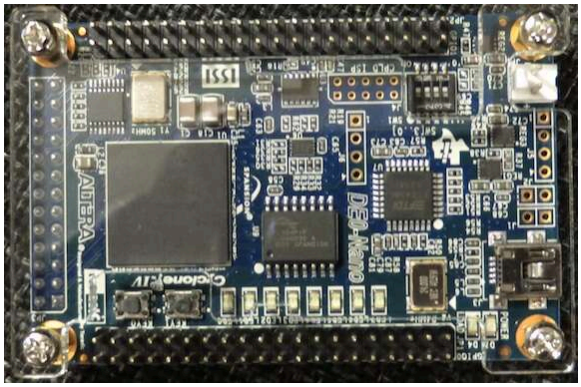


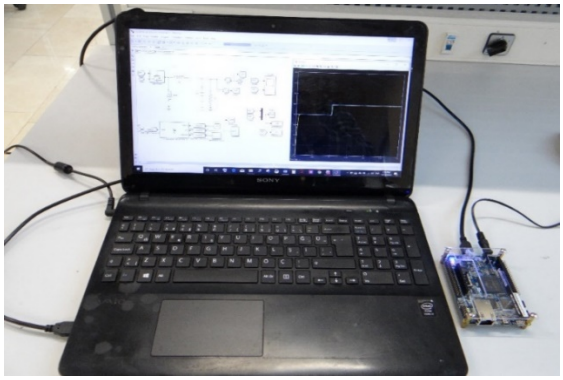
Figure 4.5. Voltage and Power of CPL

4.1.2. Co-simulation of FLC using FIL

The implementation of suggested work uses the DE0-Nano-SoC Altera FPGA board (see Figure 4.6. a., and b) and Matlab/Simulink to achieve the Verilog HDL implementation of the fuzzy logic control for DC-DC buck converters.



(a) DE0-Nano-SoC Altera FPGA board



(b) FPGA in the loop.

Figure 4.6. Co-simulation test

After the Verilog HDL module generated, the FIL Wizard will open the command window. The generated block can be replaced with FLC in Matlab/Simulink. The Simulink model modified by replacing FLC by a generated block from the HDL coder (see Figure 4.2. and Figure 4.7).

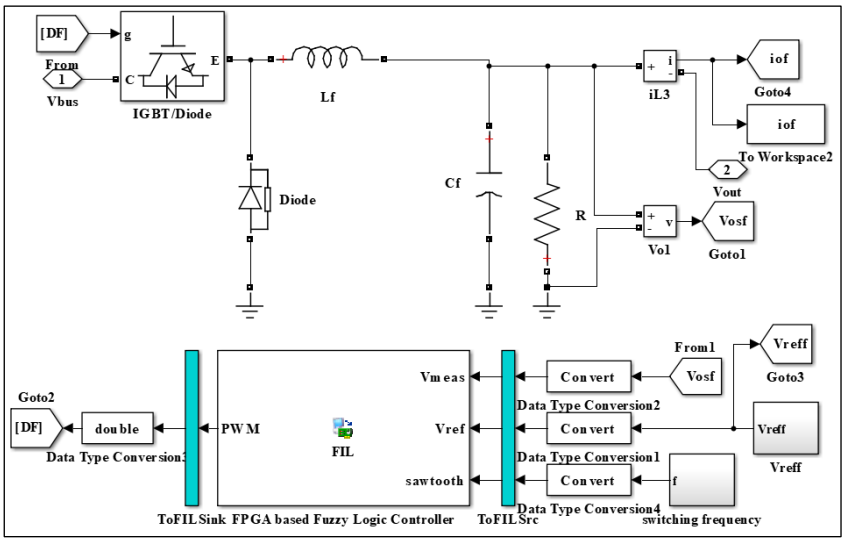


Figure 4.7. Source converter with the FLC using FPGA-in-the loop

Step voltage test

The step voltage command is designed by changing from 60-80-100 volt with 0.1 second period time, and the results for the output voltage of FLC using Matlab toolbox and FIL are shown in Figure 4.8. The output voltage using the FIL is the same response of output voltage using the Matlab toolbox. Also, for current and voltage of load converter in Co-simulation have the same outputs using Matlab toolbox, as shown in Figure 4.8. a and b.

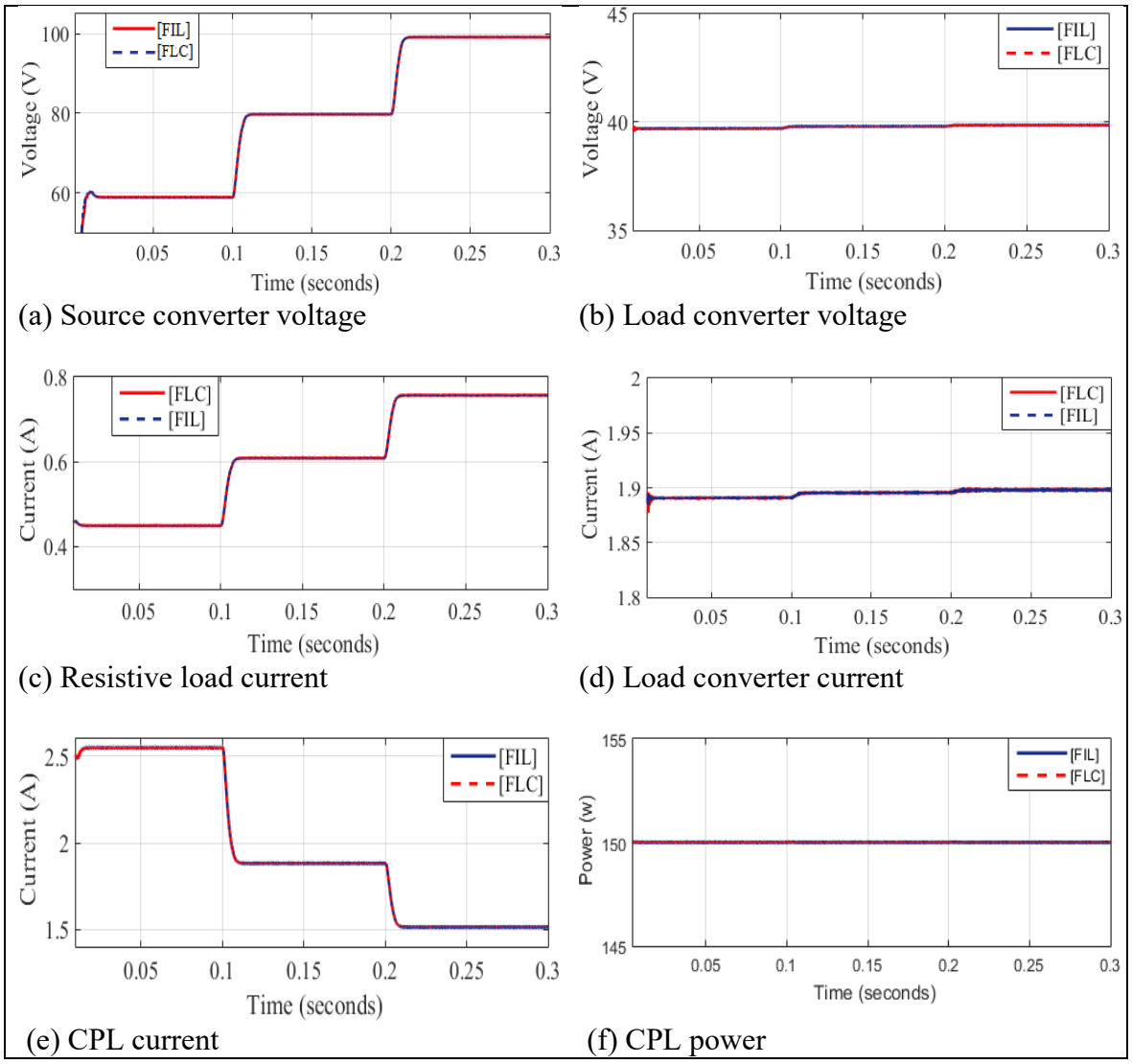
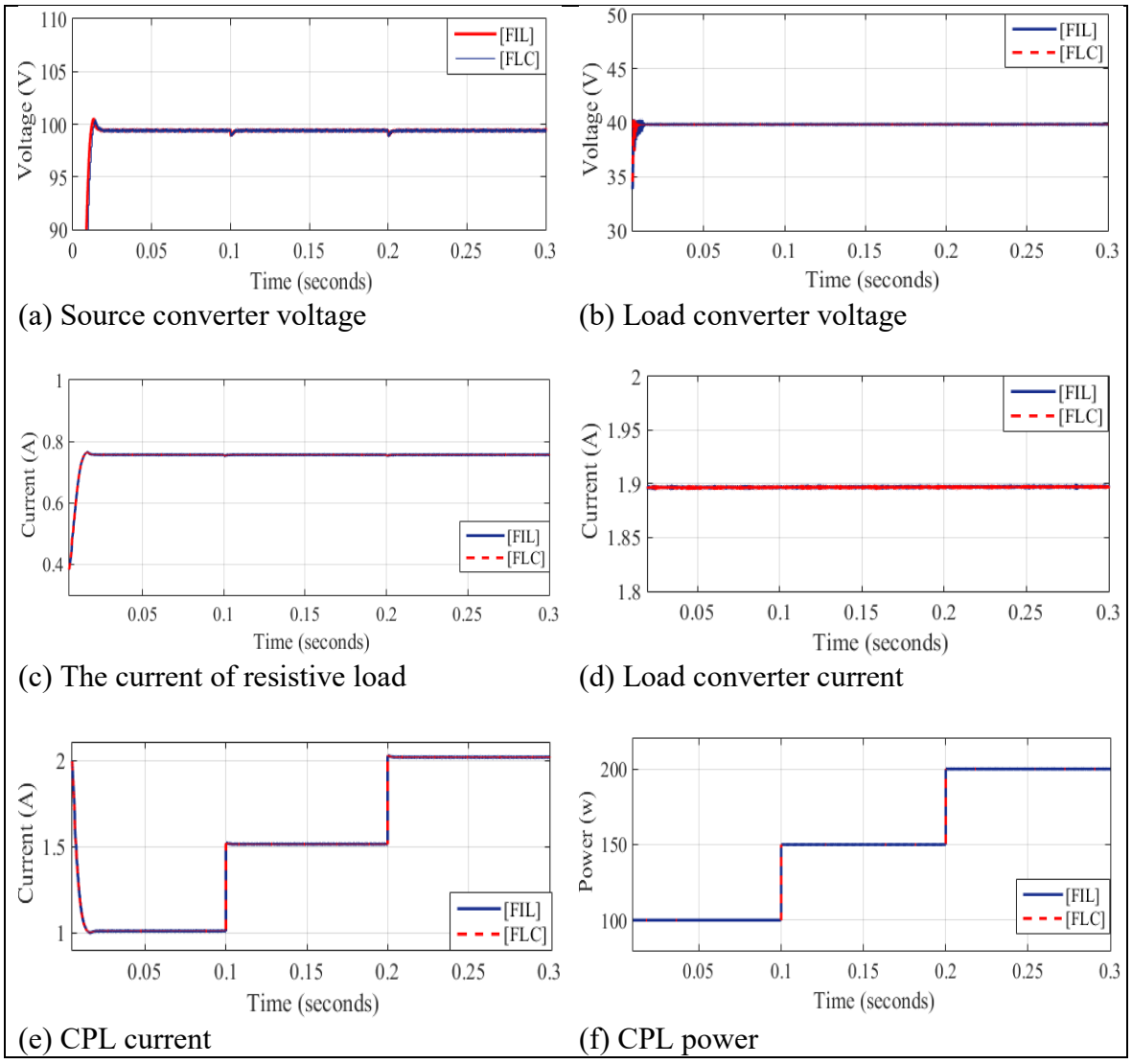


Figure 4.8. Voltage step-changing of source converter

Step power test

Herein, the step power command is designed by changing the power of the CPL from 100-150-200, as shown in Figure 4.9a. Figure 4.9 is shown the comparison between the Matlab/Simulink and FIL. The same results have been obtained.



(a) Source converter voltage
(b) Load converter voltage
(c) The current of resistive load
(d) Load converter current
(e) CPL current
(f) CPL power

Figure 4.9. Power step-changing of CPL

Step voltage reference test of load converter

In this section, the step power command is designed by changing the voltage reference of the load converter from 30-40-30 volts, as shown in Figure 4.10. The changing in reference

voltage of the load converter causes the overshoot and undershoot in all systems for a short time, but the FLC does not allow the system to go to an unstable case.

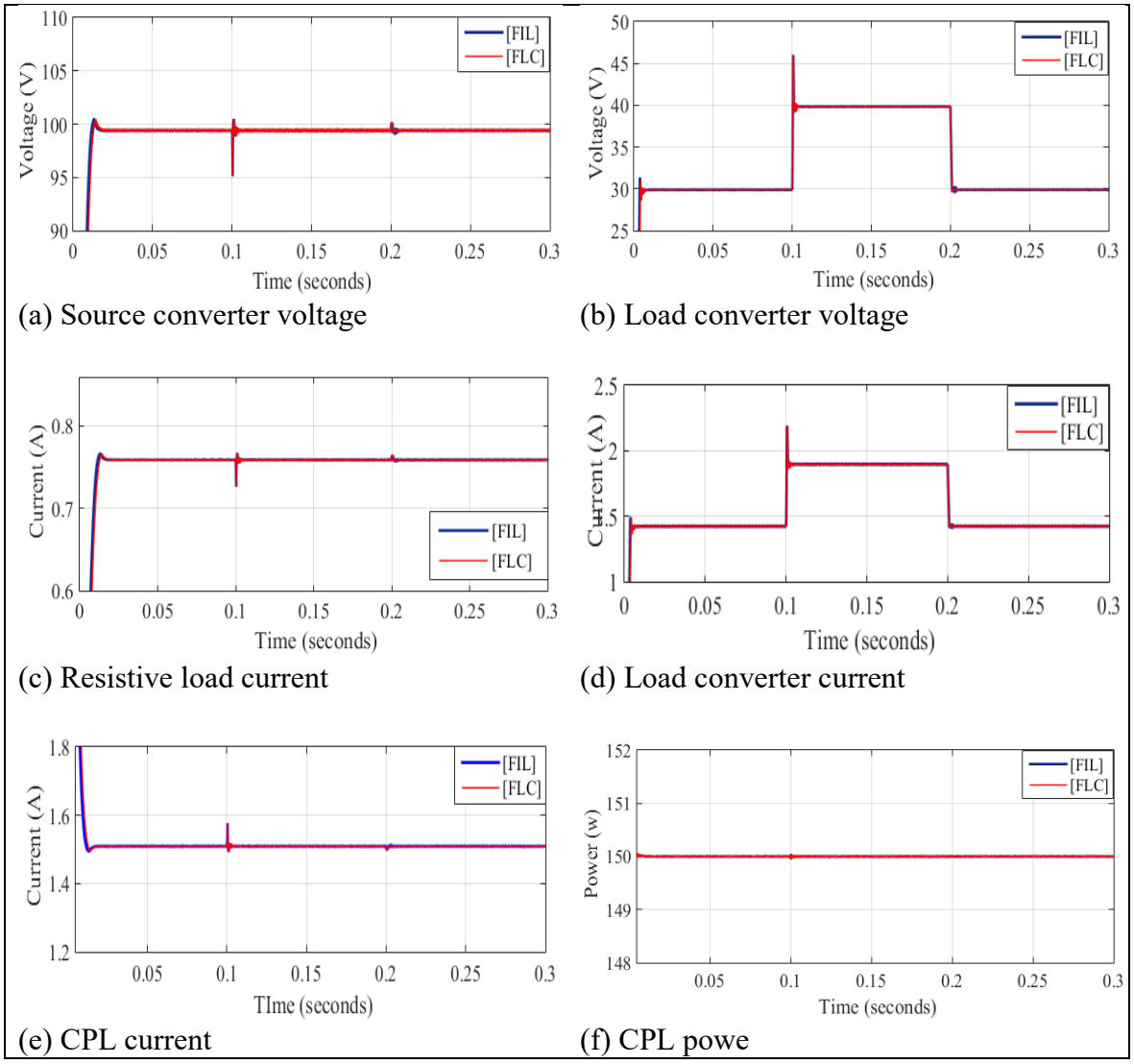
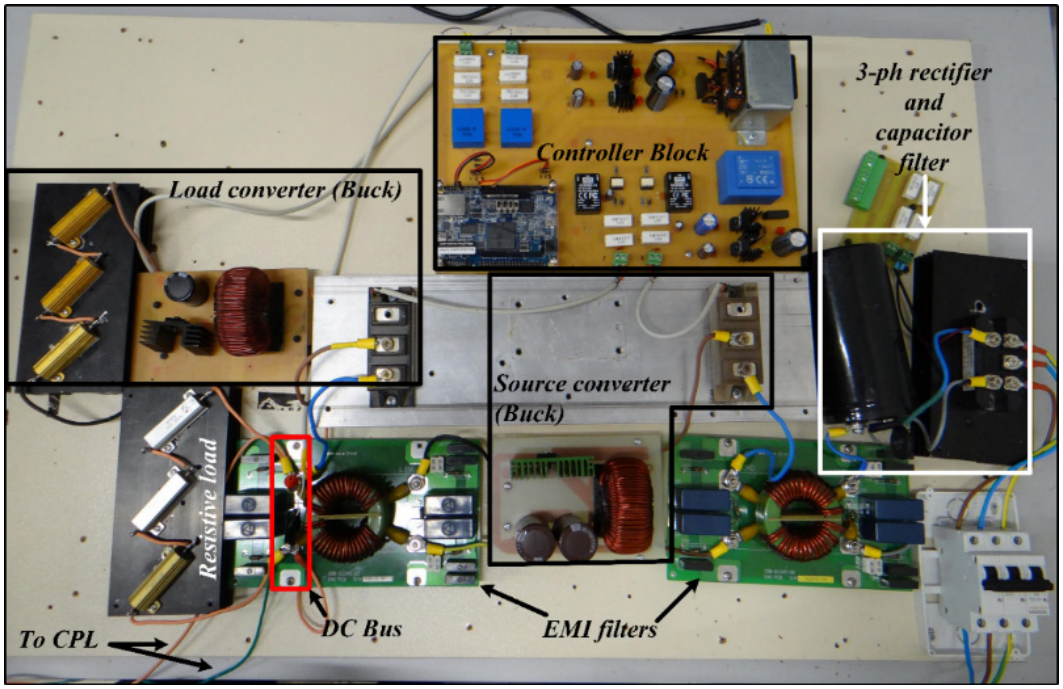


Figure 4.10. Step changing of load converter

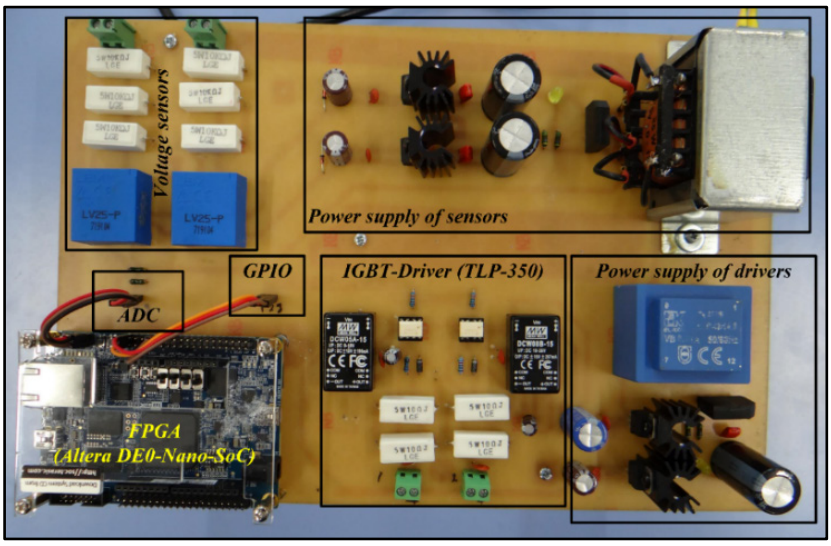
4.2. Experimental Results

In this section, the experimental results for the overall system that is shown in Figure 4.11. The two types of the controller (FLC and PI controller) is applied, and results are obtained. The Verilog HDL for controllers, clock, and PWM codes (see the index and Figure 4.12.). The same tests in simulations are applied in this section. A DC-DC buck converter is used for source and load converters. The TLP-350 are used for IGBT driver. The TLP-350 is used to isolate the control and power circuit and to provide the IGBT module required ON/OFF

switching. The DE0-Nano-SoC Altera board to implement the controller strategy. Also, the EMI filter is used to remove the conducted interference and improve the measurements sensing. Rigol DL-3021 is used as a dc power electronic (CPL) with main specifications (voltage=150 volt, current=40 Amp, and power =200 watt), as shown in Figure 4.11d.

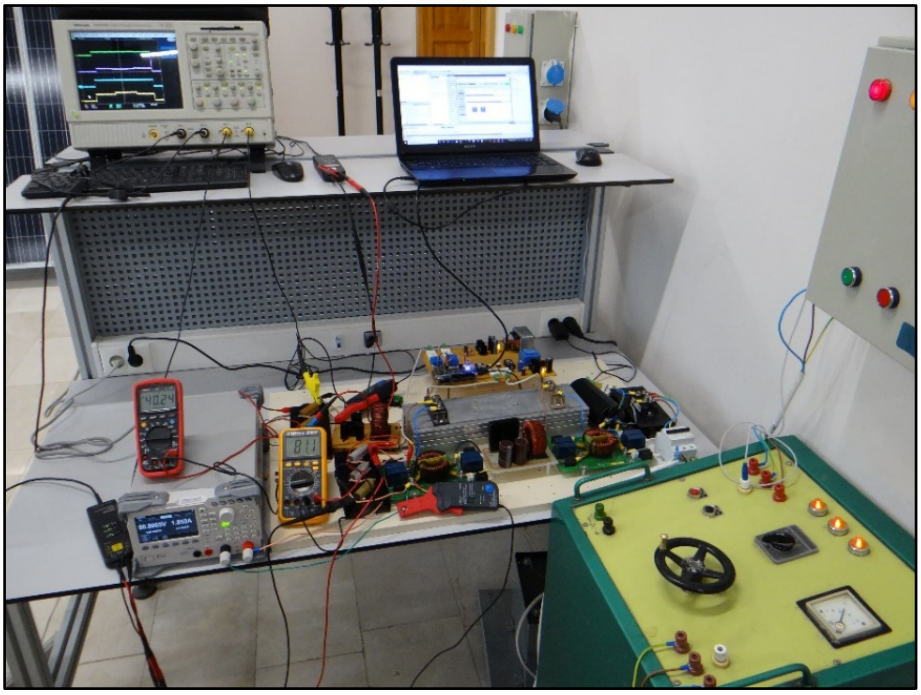


(a) Designed circuit layout

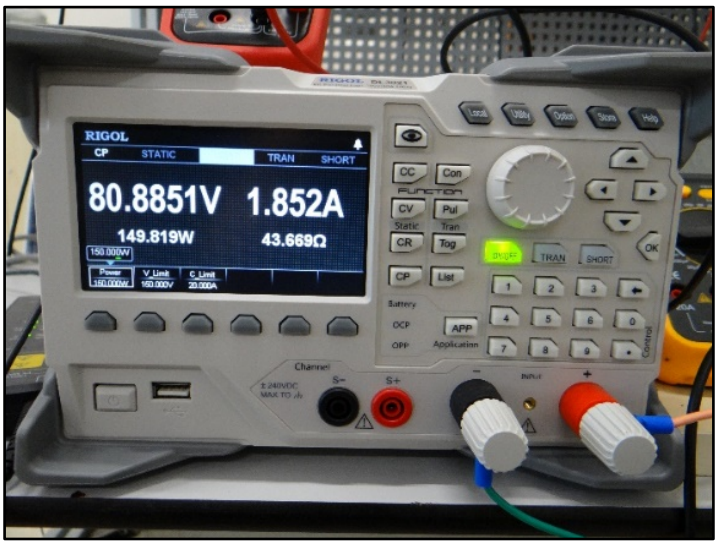


(b) Designed control board

Figure 4.11. The overall system



(c) The overall system under experimental tests



(d) Rigol DL-3021.

Figure 4.1. (Continue) The overall system

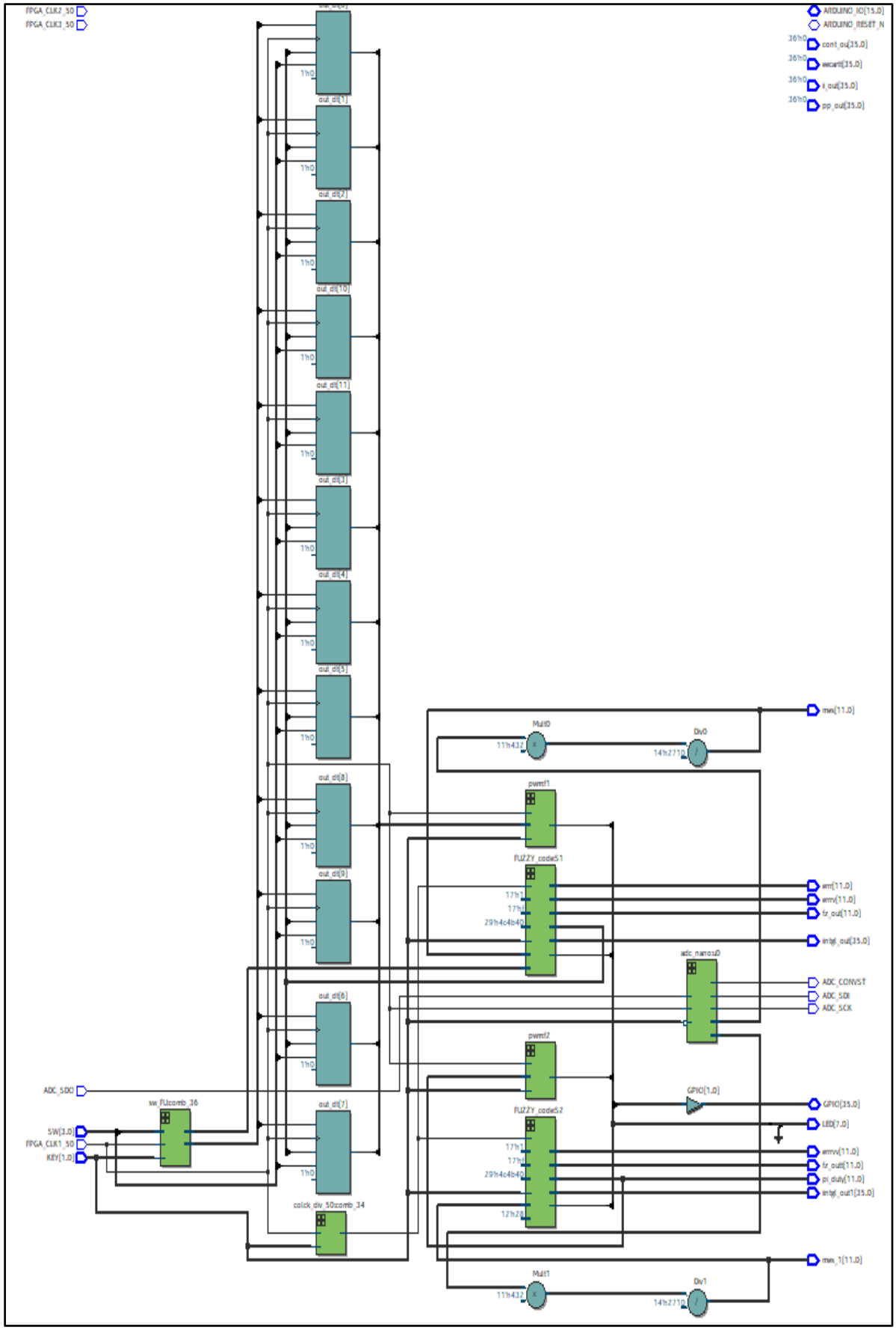


Figure 4.12. RLT of proposed controllers

Step voltage test

The first test in experimental tests is the step-changing of reference voltage for source converter. The step command is (60-80-100) volts (see Figure 4.13). The CH1 (brown color) is represented as the output voltage of the source converter (V_S). However, the output voltage is following its reference value. The CH2 (blue) and CH4 (green) are output voltage (V_L) and current (I_L) of load converter. They are fixed and stable, which means their value doesn't affect by variations of main DC-bus. The CH3 (violet) is a current of constant power load (I_{CPL}). This current decreases as the voltage of the source converter increase. The main DC-bus (V_S) does not affect, and its value is stable and has a good response.

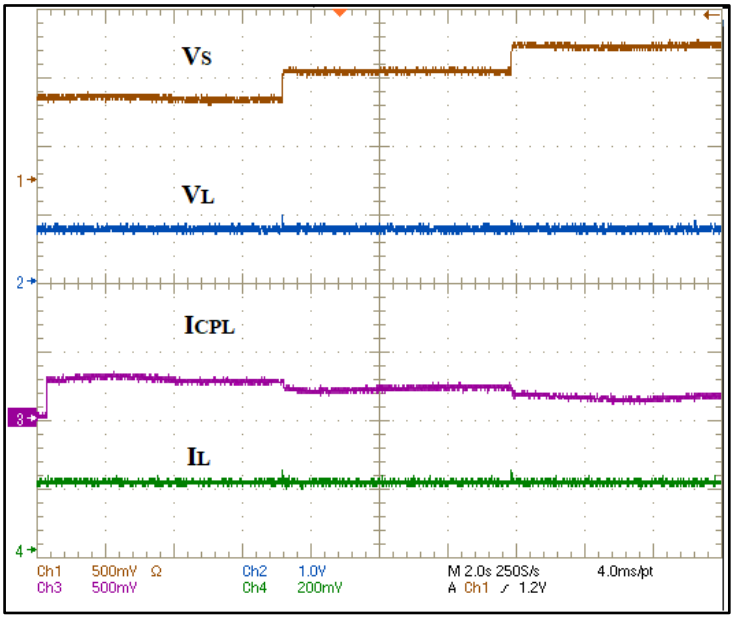


Figure 4.13. Step-changing of reference voltage for source converter

Comparison between experimental and simulation results

Herein, the Comparison between experimental and simulation results are introduced. These results are concluded form the step-changing of reference voltage for source converter (see Figure 4.14). The experimental results are similar to simulation results. Figure 4.14a and b have the same response to reference value (60-80-100) volts. Also, the voltage of the load converter is about 40 volts in Figures 4.14c and d. the CPL current has the same figure, and current values as (2.5-1.9-1.5) for step voltage (60-80-100) with CPL power is 150 watts (see Figure 4.14g and h).

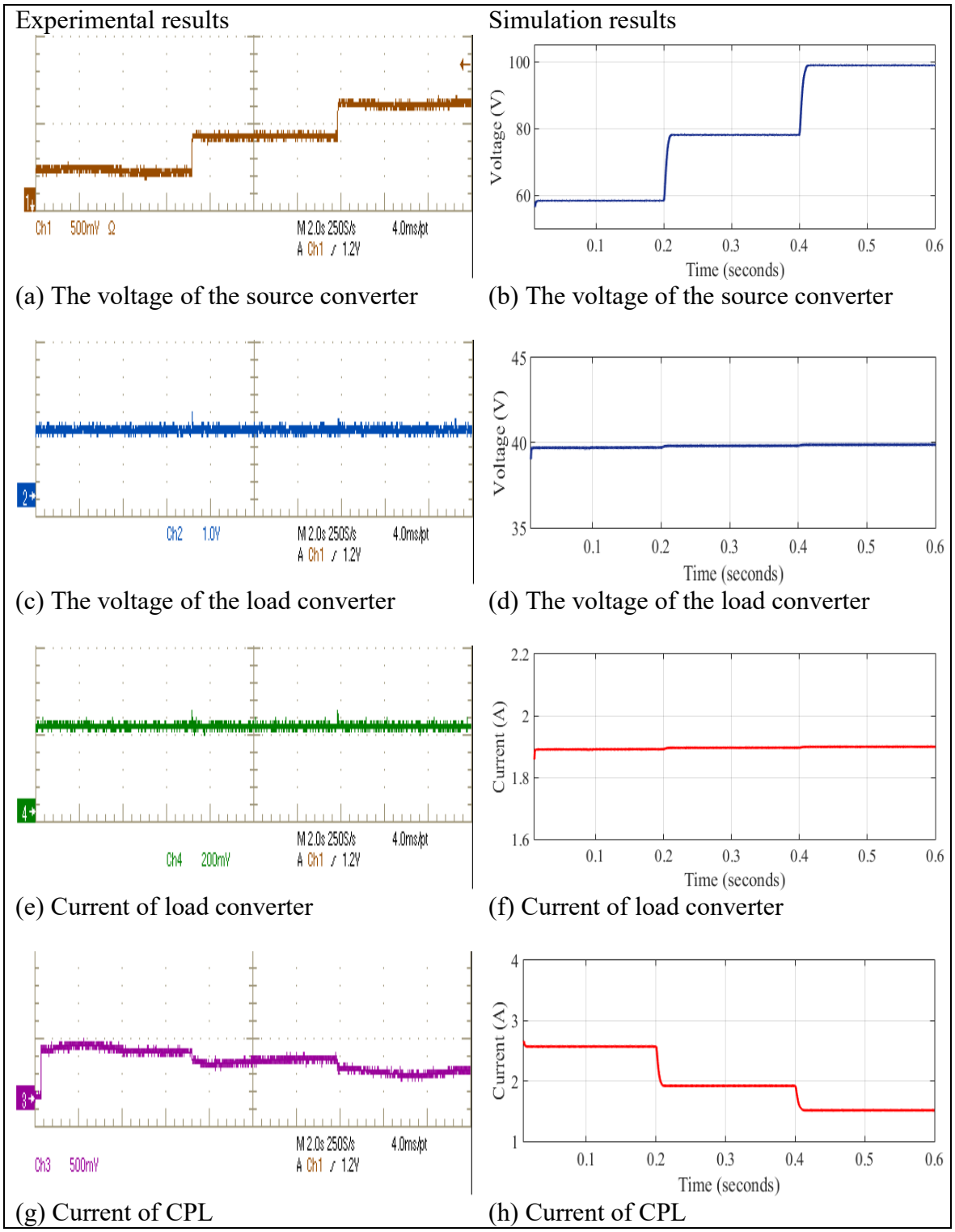
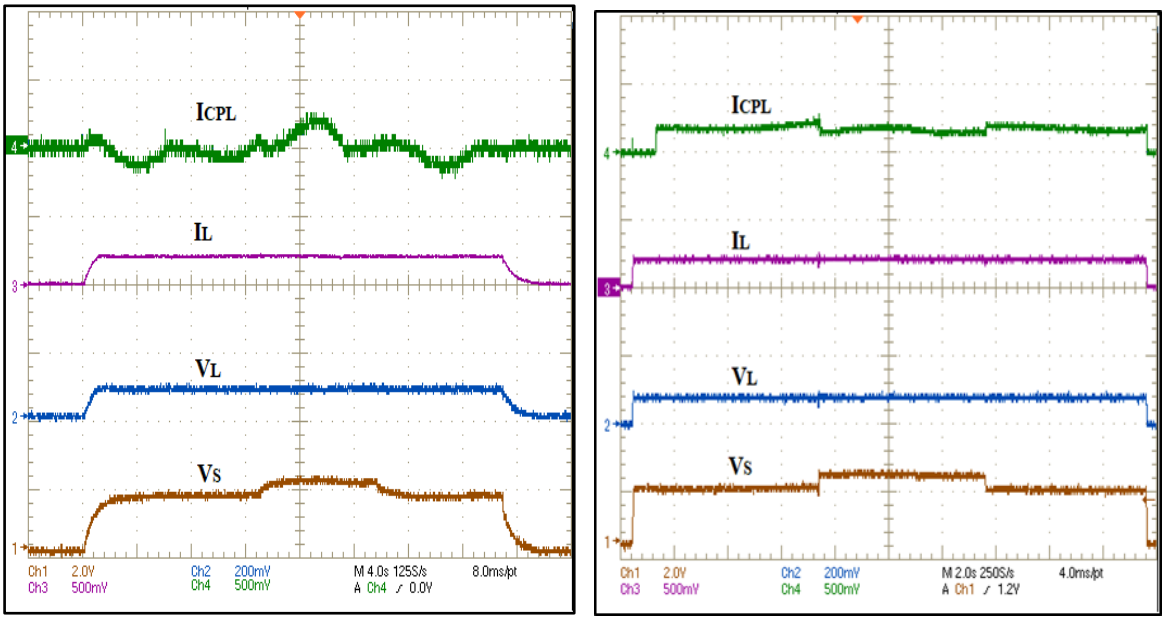


Figure 4.14. Comparison between experimental and simulation results

Comparison between FLC and PI controller

Figure 4.15a shows the overall system under the PI controller and Figure 4.15b for FLC. The voltage of the source converter (V_S) of PI and FLC has matched the reference value of

voltage (80-100-80) volts without overshoot. The CPL current (I_{CPL}) is not stable in Figure 4.15a and has oscillations while the current is stable and constant in Figure 4.15b.



(a) PI controller (b) FL controller

Figure 4.15. Comparison between PI and FL controllers for source converter

FLC under multiple tests

The FLC is applied on the load converter with step changing of voltage reference (30-40-30) volt with source converter voltage (V_S=100 volts), and P_{CPL} is 100 watts. The voltage of the load converter (V_L) under FLC more stable without overshoot or undershoot in current and voltage of load converter and follows the reference value with good response, as shown in Figure 4.16b. (CH2 for voltage (V_L) and CH4 for current (I_L)). Also, the voltage transient at load converter did the effect on DC main bus that feeding by source converter. The current of constant power load (I_{CPL}) is stable as a result of the stabilization of source converter voltage.

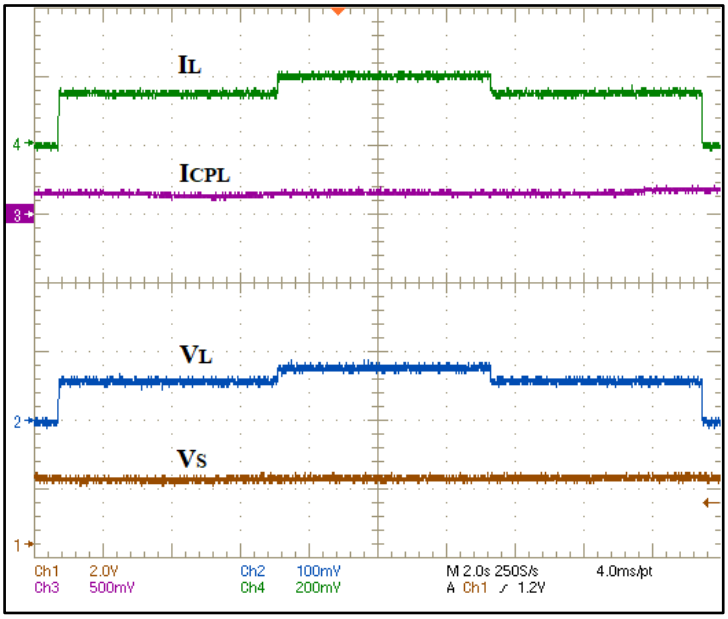


Figure 4.16. Voltage step-changing of controllers for load converter

In this section, multiple tests have been done on the system under FLC. The first test is removed from the CPL and load converter, as shown in Figure 4.17. The system has only resistive, and voltage step-changing is applied (80-100-80) volts. The system has a fast and stable response and loads current take form of the input voltage.

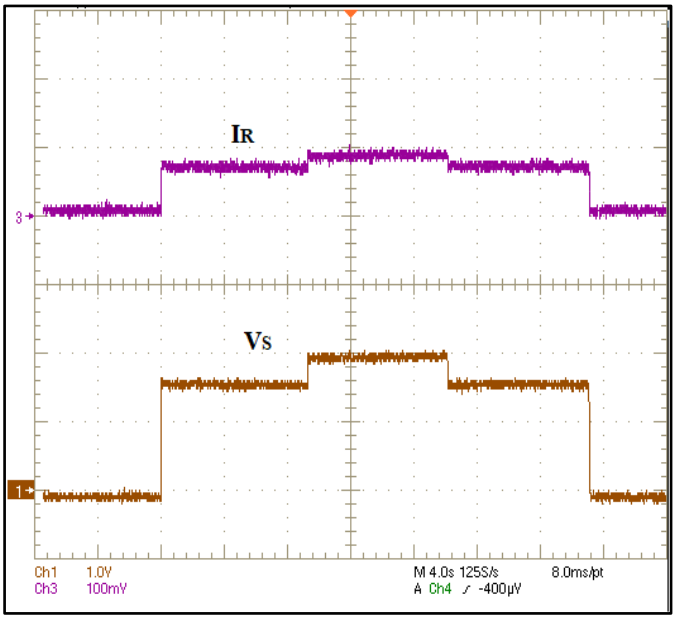


Figure 4.17. Source converter with resistive load

Figure 4.18. is illustrated the system with CPL and resistive load. As shown from the same step-changing of source converter voltage applied. Also, the current resistive load increases/decrease as the output voltage of source increase/decrease as a linear relationship between voltage and current in resistor according to Ohm law's (see Figure 4.18. CH2). In otherwise, the CPL current increase/decrease when the output voltage of source decreases/increases as mention in the concept of constant power load and its incremental negative resistance. The voltage did not affect by incremental negative resistance instability effects. The FLC has forced the output of the source converter to follow its reference value, and bring it to the steady-state case.

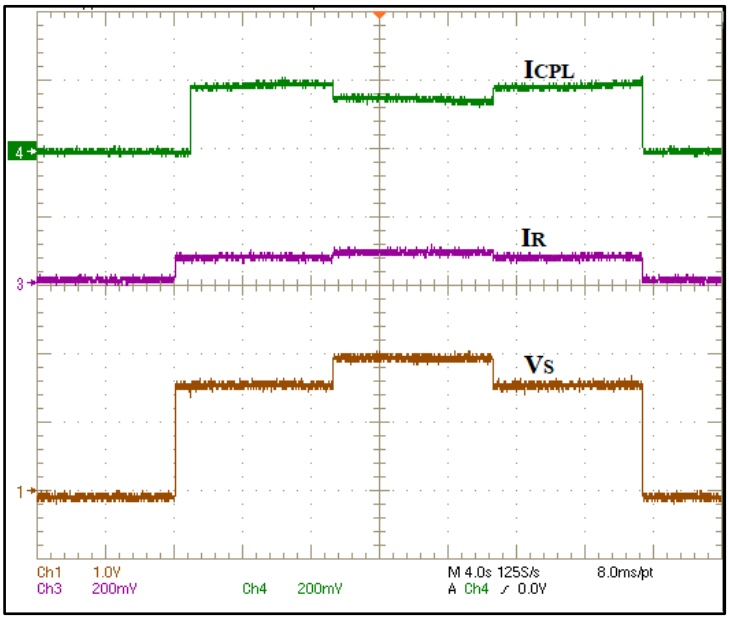


Figure 4.18. Source converter with CPL and resistive load

Figure 4.19. shows the results of the load converter and resistive load. The step-changing is applied to source converter voltage, and load converter voltage saves at 40 volts. The output voltage and current at the voltage load converter terminal are kept constants and stable during variations of source converter voltage. The voltage and current of resistive load are varied as the voltage is change.

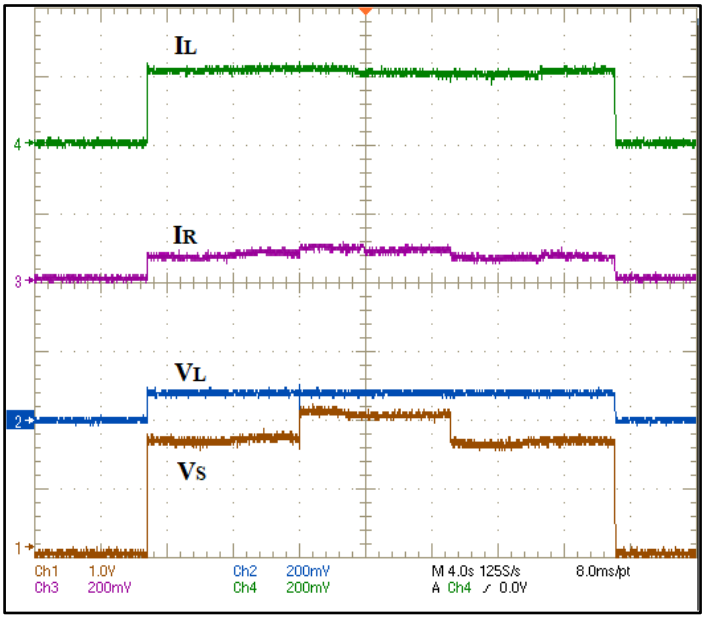


Figure 4.19. Source converter with load converter and resistive load

Figures 4.20. and 4.21. shows the load variations in the resistive load that is changing as (131-57-131) Ohm with 150 watts for CPL and source voltage 100 volts. The voltage of the source converter did not affect by the change of load also for CPL current is still stable, and the same value without oscillation during the load step up or down.

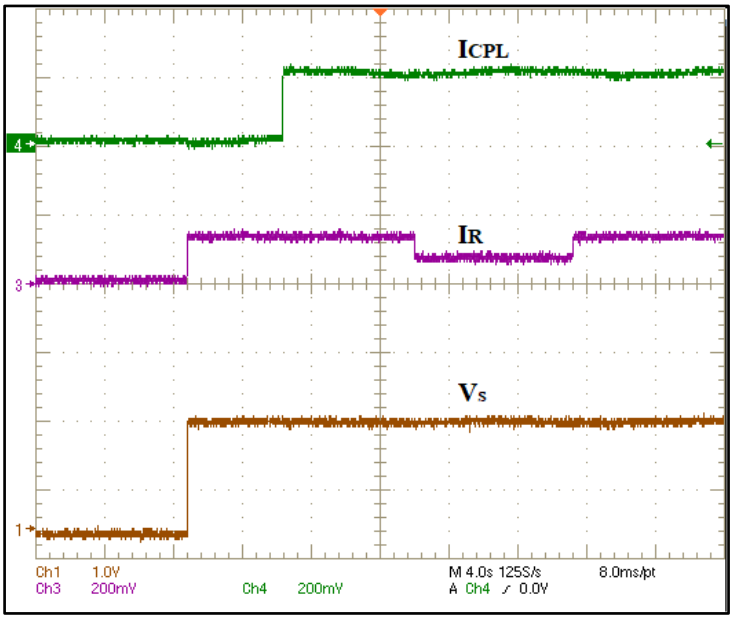


Figure 4.20. Step changing in a resistive load

Figure 4.21. is included the On/Off switching test of CPL with 150 watts, the resistive load is 130 Ohm, and the voltage of the source and load converter is 100 and 40 volts, respectively., as shown in Figures 4.20, 4.21.

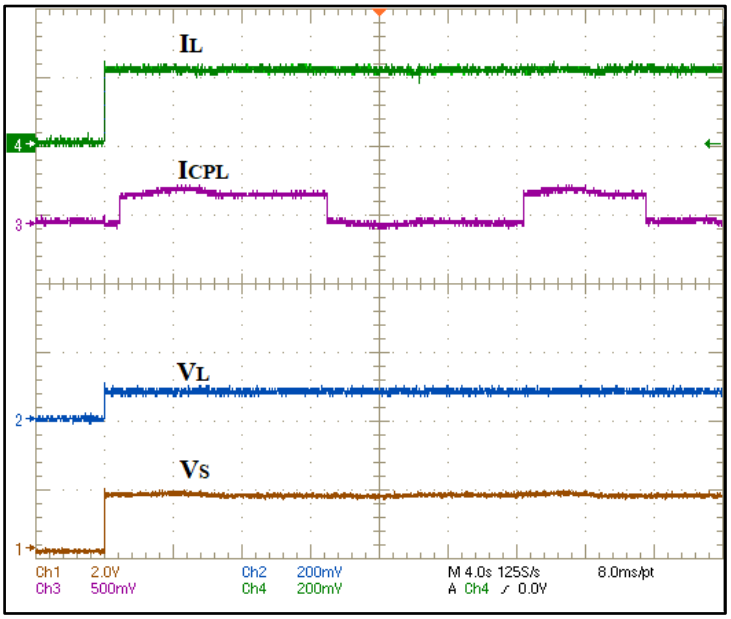


Figure 4.21. On/Off switch of CPL

The dc bus of three-phase rectifier has been saved at a constant value with droop voltage (8 volts), as illustrated 4.22.

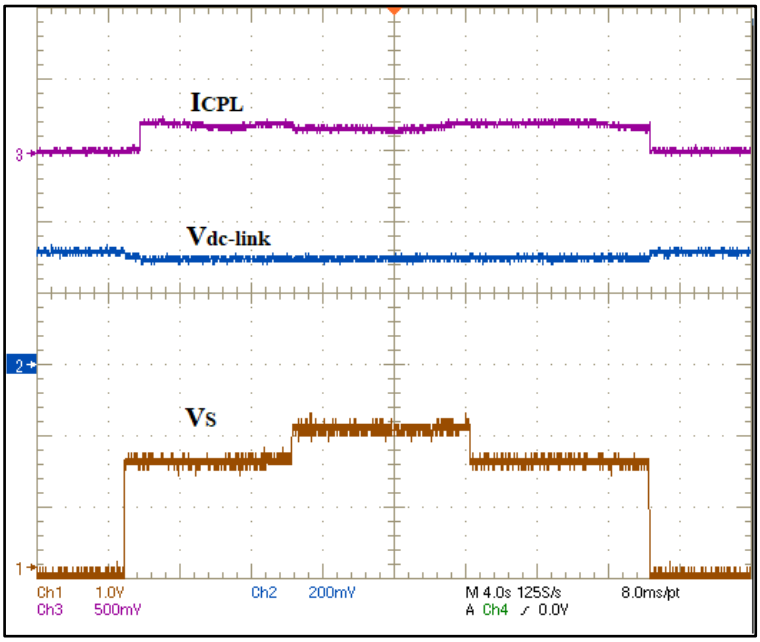


Figure 4.22. DC-bus of 3-ph rectifier CH2

Summary of experimental results

These successive figures reveal the following results: the designed FLC has saved and regulated the output voltage of source converter without oscillations in voltages and currents of the different types of load under load variations. The result presented a proper voltage following response and matched the reference value of voltage. Also, FLC has had a good response with nonlinear load and prevents propagating the instability effects in the system.

5. CONCLUSION

The main motivation for this thesis was the increased use of electronic devices, power electronic converters, and their various structures and connection types for different applications in the DC distributed power system.

In this thesis, the fuzzy logic control (FLC) is introduced as a new suggestion control for a DC-DC multi converter system with a constant power load. The multi converter has different type of loads (i.e. resistive load, constant power load, and DC-DC buck converter) with single source converter (DC-DC buck converter). The applied fuzzy logic control algorithm was verified by using simulation and experimental tests.

The simulation results have Matlab toolbox and FPGA in the loop tool. The comparisons have been among results that are gotten from the simulations and verification under various tests. The Matlab/Simulink has been used to achievement the proposed controller, which demonstrated results. The resulting fuzzy logic controller has been found as robust and efficient. The output voltage of the buck converter matches the reference value of voltage before and after the step-changing in the reference voltage and load variation conditions.

Also in this work has been successfully introduced a voltage control and stabilization by using the fuzzy logic control for DC-DC buck converter drive and demonstrated its performance from co-simulation to FPGA realization. The fuzzy logic control has been programmed in Verilog HDL. After this, fuzzy logic control is implemented in the DE0-Nano-SoC Altera FPGA board. During the modeling, the co-simulation between the FLC toolbox and the Verilog HDL model is done.

Experimental results have been obtained by using the DE0-Nano-SoC Altera FPGA board and Verilog HDL codes for PI controller, FLC, PWM, and clock divider. The DC-DC buck converter is constructed for load and source converter. An IBGT driver is also built based on TLP-350.

The experimental results using a fuzzy logic controller can be summarized as follows:

- Compared to passive damping methods, the fuzzy logic has the best efficiency because does not need to add or resize the passive elements like resistor, inductor, and capacitor that are added the losses to the system.
- Compared to active damping mothed, the fuzzy logic controller did not make a drop in output voltage.
- Compared Pulse Adjustment Control Technique, the fuzzy logic controller, has low output voltage ripple, noise, and the sub-harmonic presented at the output voltage.
- Compared Sliding Mode Control, the fuzzy logic controller is capable at a high voltage and low voltages

The experimental result shows the FLC is more efficient compared to the PI controller against system variation such voltage step-up/ down or load variations and has quick response to regulate output and keep it at the desired value without oscillations. Also, the Fuzzy logic has a good response to step changes in voltage response compared to the PI controller.

The multiple experimental tests are done. The fuzzy logic controller guarantees the stabilization of the buck converter anti destabilizing effect of CPL and also ensures the tight voltage regulation.

In this thesis we only used single unit of source converter at first stage of multiconverter. The first stage can use some improvement by adding two or more source converters.

Although the two type of constant power load can exist at DC distributed power system, we studied the behavior of DC constant power load and its effects on the system. Hence, we will discuss and analysis the stability of AC-CPL. All types of motor drivers can be represented as AC-CPL, for this aim will use the Fuzzy-PI controller. The Fuzzy controller will use for tuning the PI parameters.

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Publications

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2. AL-Nussairi, M.K., Bayindir, R., Padmanaban, S., Mihet-Popa, L., Siano, P. (2017). Constant power loads (CPL) with microgrids: Problem definition, stability analysis and compensation techniques. Energies Journal, 10(1656), 1-20.

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